



QuickSwitch™ Literature Package

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QuickSwitch™ Literature Package Contents

- **QuickSwitch™ Data Sheets:**

QS54/74QST3383

QS54/74QST3583 (preliminary)

QS54/74QST3384

QS54/74QST3584 (preliminary)

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High Speed CMOS Bus Exchange Switches

QS54/74QST3383
QS54/74QST3583
(3583 PRELIMINARY)

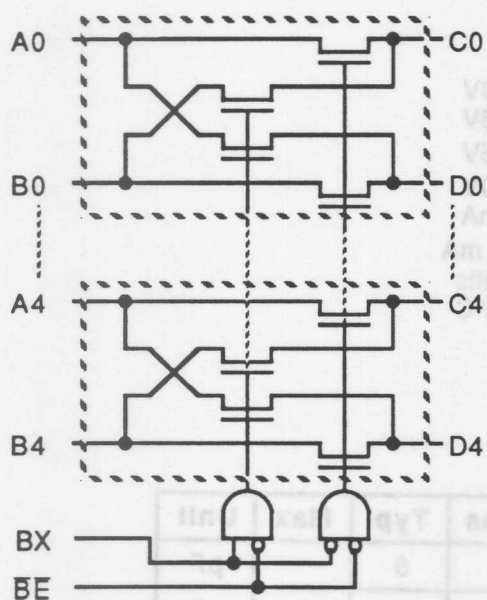
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Direct bus connection when switches on
- Zero propagation delay (3383)
- Undershoot Clamp diodes on all inputs
- Low power CMOS proprietary technology
- 3583 is 25Ω version for low noise
- Bus exchange allows nibble swap
- Zero ground bounce in flow-through mode
- TTL-compatible input and output levels
- Available in 24-pin DIP, ZIP, SOIC and QSOP

DESCRIPTION

The QS54/74QST3383 and 3583 each provide two sets of ten high-speed CMOS TTL-compatible bus switches. The low on resistance (5Ω) of the 3383 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The 3583 adds an internal 25Ω resistor to reduce reflection noise in high speed applications. The bus enable (BE) signal turns the switches on. The bus exchange (BX) signal provides nibble swap of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters, etc.

FUNCTIONAL BLOCK DIAGRAM



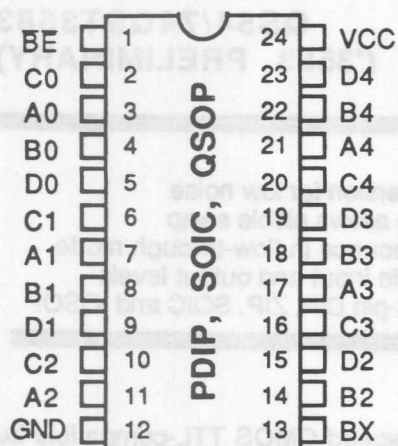
PIN DESCRIPTION

Name	I/O	Function
A0-4, B0-4	I/O	Buses A, B
C0-4, D0-4	I/O	Buses C, D
BE	I	Bus Switch Enable
BX	I	Bus Exchange

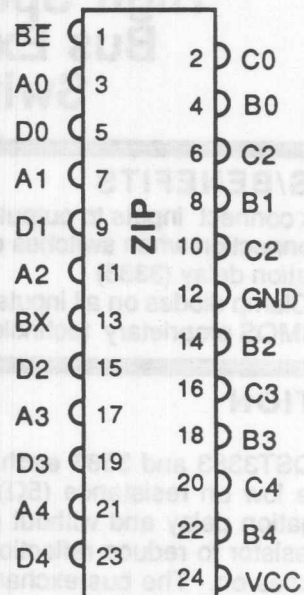
FUNCTION TABLE

BE	BX	A0-4	B0-4	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C0-4	D0-4	Connect
L	H	D0-4	C0-4	Exchange

PIN CONFIGURATIONS



ALL PINS TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Switch Voltage V_S	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Current Max. sink current/pin.....	120 mA
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0V$, $V_{out} = 0V$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance, Controls	$V_{in} = 0V$	6		pF
Coff	A/B I/O Capacitance, Switch Off	$V_{in} = 0V$	6		pF
Con	A/B I/O Capacitance, Switch On	$V_{in} = 0V$	10		pF

Capacitance is guaranteed but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

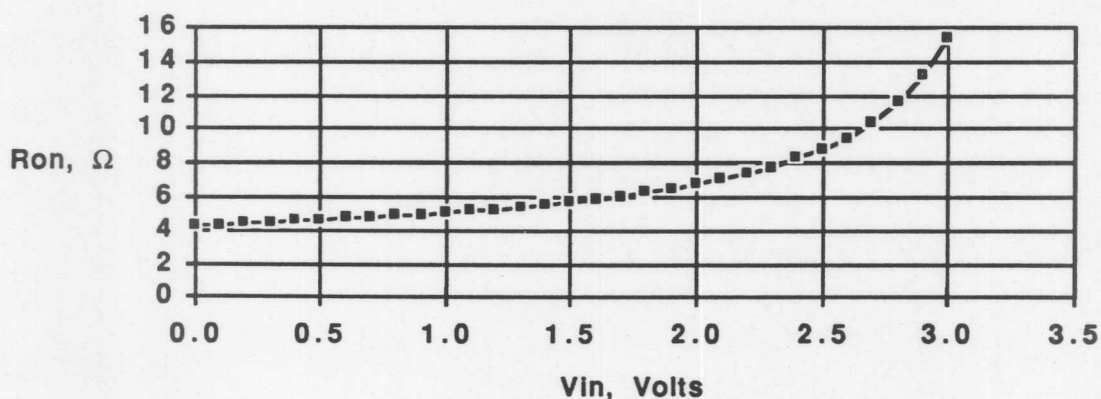
Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Vih	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	-	-	Volts
Vil	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	-	-	0.8	Volts
lin	Input Leakage Current	0 ≤ Vin ≤ Vcc	-	-	1	μA
loz	Off State Current (Hi-Z)	0 ≤ A, B ≤ Vcc	-	.001	1	μA
los	Short Circuit Current (2)	A (B) = 0V, B (A) = Vcc	100	-	-	mA
Vic	Clamp Diode Voltage	Vcc = Min, lin = -18 mA	-	-0.7	-1.2	Volts
Ron	Switch On Resistance (Notes: 3,4)	Vcc = Min, Vin = 0.0 Volts Ion = 48 mA	33XX	-	5	7 Ω
			35XX	24	28	35 Ω
		Vcc = Min, Vin = 2.4 Volts Ion = 15 mA	33XX	-	10	15 Ω
			35XX	24	35	48 Ω

Notes:

1. Typical values indicate VCC=5.0V and TA=25°C.
2. Not more than one output should be used to test this high power condition, and the duration is ≤1 second.
3. Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A, B) pins.
4. 35xx Ron is a preliminary specification.

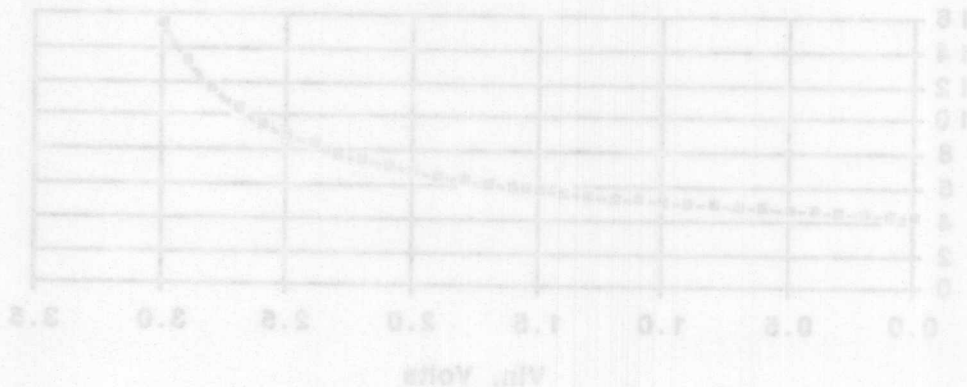
On Resistance vs Vin @ 4.75 Vcc (338X Only)



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Typ	Max	Unit
I_{cc}	Quiescent Power Supply Current	$V_{cc} = \text{MAX}, V_i = \text{GND or } V_{cc}, f = 0$	-	-	1.5	mA
ΔI_{cc}	Pwr Supply Current, per Input High (2)	$V_{cc} = \text{MAX}, \text{Input} = 3.4 \text{ V}, f = 0$ Per control input	-	-	2.5	mA
Q_{ccd}	Dynamic Pwr Supply Current per mHz (3)	$V_{cc} = \text{MAX}, \text{A \& B pins open},$ Control input toggling @ 50% duty cycle	-	-	0.25	mA/mHz
I_c	Total Power Supply Current (4,5)	$V_{cc} = \text{MAX}, \text{A \& B pins at } 0.0\text{V},$ Control inputs toggling @ 50% duty cycle $V_{ih} = 3.4\text{V}, f_{\text{clock}} = 10 \text{ mHz}$	-	-	9.0	mA

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_i=3.4\text{V}$, control inputs only). A and B pins do not contribute to I_{cc} .
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
- $I_c = I_{\text{Quiescent}} + I_{\text{Inputs}} + I_{\text{Dynamic}}$
 $I_c = I_{cc} + \Delta I_{cc} Dh Nt + Q_{ccd} (fi Ni)$
 I_{cc} = Quiescent Current
 ΔI_{cc} = Power Supply Current for each TTL High input ($V_i=3.4\text{V}$, control inputs only)
 Dh = Duty Cycle for each TTL input that is High (control inputs only).
 Nt = Number of TTL inputs that are at DH (control inputs only).
 fi = frequency that the inputs are toggled (control inputs only).
- Note that activity on A and/or B inputs do not contribute to I_c if A and B inputs are between gnd and V_{cc} . The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, I_c will be equal to I_{cc} only regardless of activity on the A and B pins.



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Note	Com		Mil		Unit
			Min	Max	Min	Max	
† PLH † PHL	Data Propagation Delay Ai to Bi, Bi to Ai	338X 2,3		0.25		0.25	ns
		358X 2,3,7		1.25		1.25	ns
† PZH † PZL	Switch Turn On Delay BE to Ai, Bi	338X 1	1.5	6.5	1.5	7.5	ns
		358X 1,7	1.5	7.5	1.5	8.5	ns
† PLZ † PZL	Switch Turn Off Delay BE to Ai, Bi	338X 1,2	1.5	5.5	1.5	6.5	ns
		358X 1,2,7					
† BX	Switch Multiplex Delay BX to Ai, Bi	338X 1	1.5	6.5	1.5	7.5	ns
		358X 1,7	1.5	7.5	1.5	8.5	ns
Qci	Charge Injection, Typical	338X 4,6		1.5		1.5	pC
		358X 4,6,7					
Qdci	Differential Charge Injection, Typical	338X 5,6		<.5		<.5	pC
		358X 5,6,7					

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and aloa alone is of the order of 0.25 ns for 50 pf load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- 4) Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts.
- 5) Measured at switch turn off through bus multiplex, A to C => A to D, B connected to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.
- 6) Characterized parameter. Not 100% tested.
- 7) Preliminary data, subject to change.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, VCC = 5.0V to 5.5V, VEE = 0V to -5.5V, unless otherwise noted.
 Military TA = -55°C to 125°C, VCC = 5.0V to 5.5V, VEE = 0V to -5.5V, unless otherwise noted.

Symbol	Description	Notes	Com		Mil		Unit
			Min	Max	Min	Max	
1PLH	Data Propagation Delay	338X		0.25		0.25	ns
1PLL	A to B, B to A	358X		1.25		1.25	ns
1PLH	Switch Turn On Delay	338X	1.5	8.5	1.5	7.5	ns
1PLL	B to A, B	358X	1.5	7.5	1.5	8.5	ns
1PLS	Switch Turn Off Delay	338X	1.5	8.5	1.5	8.5	ns
1PLL	B to A, B	358X	1.5	7.5	1.5	8.5	ns
1BX	Switch Multiplex Delay	338X	1.5	8.5	1.5	7.5	ns
	B to A, B	358X	1.5	7.5	1.5	8.5	ns
1Cot	Charge Injection, Typical	338X		1.5		1.5	pC
		358X		4.0			
1CotI	Differential Charge Injection, Typical	338X		8.5		< 5	pC
		358X		2.0			

Notes:

- 1) See Test Circuit and Waveforms. Minimum guaranteed but not tested.
- 2) The parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and load time is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the typical times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- 4) Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, V_{in} at A = 0.0 volts.
- 5) Measured at switch turn off through bus multiplexer, A to C, load = 50 pF in parallel with 10 meg scope probe, V_{in} at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.
- 6) Characterized parameter. Not 100% tested.
- 7) Preliminary data, subject to change.



High Speed CMOS 10-bit Bus Switches

QS54/74QST3384
QS54/74QST3584
(*3584 PRELIMINARY)

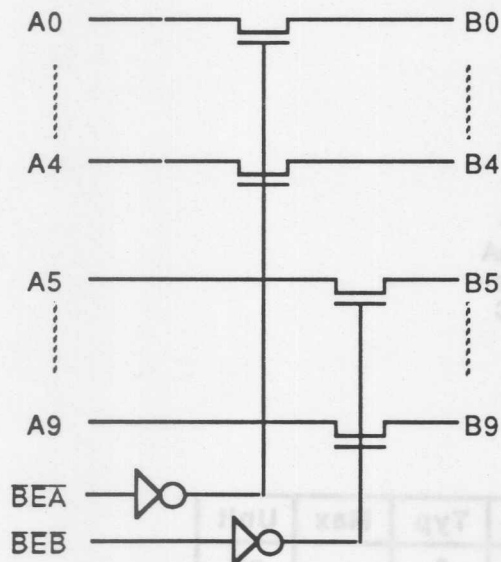
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Direct bus connection when switches on
- Zero propagation delay (3384)
- Undershoot Clamp diodes on all inputs
- Low power CMOS proprietary technology
- 3584 is 25Ω version for low noise
- Two enables control 5 bits each
- Zero ground bounce in flow-through mode
- TTL-compatible input and output levels
- Available in 24-pin PDIP, ZIP, SOIC and QSOP

DESCRIPTION

The QS54/74QST3384 and 3584 each provide a set of ten high-speed CMOS TTL-compatible bus switches. The low on resistance (5Ω) of the 3384 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The 3584 adds an internal 25Ω resistor to reduce reflection noise in high speed applications. The bus enable (BE) signals turn the switches on. Two bus enable signals are provided, one for each of the upper and lower five bits of the two 10-bit buses.

FUNCTIONAL BLOCK DIAGRAM



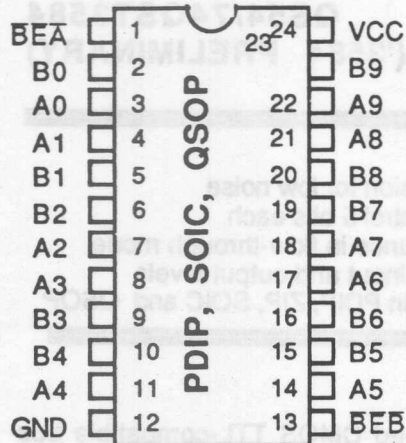
PIN DESCRIPTION

Name	I/O	Function
A0-9	I/O	Bus A
B0-9	I/O	Bus B
BEA, BEB	I	Bus Switch Enable

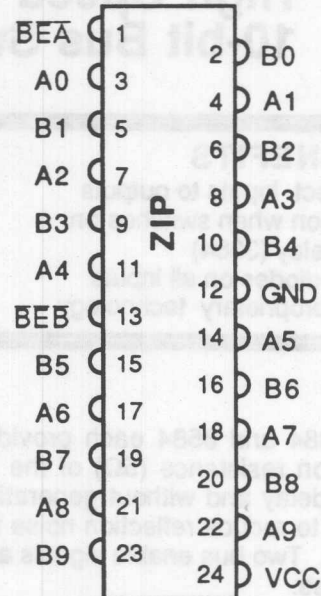
FUNCTION TABLE

BEA	BEB	B0-4	B5-9	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A0-4	Hi-Z	Connect
H	L	Hi-Z	A5-9	Connect
L	L	A0-4	A5-9	Connect

PIN CONFIGURATIONS



ALL PINS TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Switch Voltage V_S	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Current Max. sink current/pin.....	120 mA
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0V$, $V_{out} = 0V$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance, Controls	$V_{in} = 0V$	6		pF
Coff	A/B I/O Capacitance, Switch Off	$V_{in} = 0V$	6		pF
Con	A/B I/O Capacitance, Switch On	$V_{in} = 0V$	10		pF

Capacitance is guaranteed but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5%

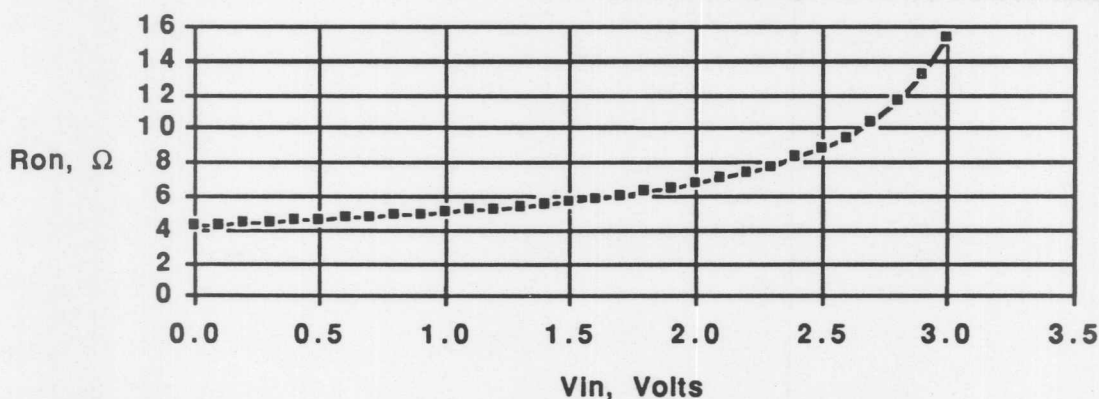
Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Vih	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	-	-	Volts
Vil	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	-	-	0.8	Volts
lin	Input Leakage Current	0 ≤ Vin ≤ Vcc	-	-	1	μA
loz	Off State Current (Hi-Z)	0 ≤ A, B ≤ Vcc	-	.001	1	μA
los	Short Circuit Current (2)	A (B) = 0V, B (A) = Vcc	100	-	-	mA
Vic	Clamp Diode Voltage	Vcc = Min, lin = -18 mA	-	-0.7	-1.2	Volts
Ron	Switch On Resistance (Notes: 3,4)	Vcc = Min, Vin = 0.0 Volts Ion = 48 mA	33XX	-	5	7 Ω
			35XX	24	28	35 Ω
		Vcc = Min, Vin = 2.4 Volts Ion = 15 mA	33XX	-	10	15 Ω
			35XX	24	35	48 Ω

Notes:

1. Typical values indicate VCC=5.0V and TA=25°C.
2. Not more than one output should be used to test this high power condition, and the duration is ≤1 second.
3. Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A, B) pins.
4. 35xx Ron is a preliminary specification.

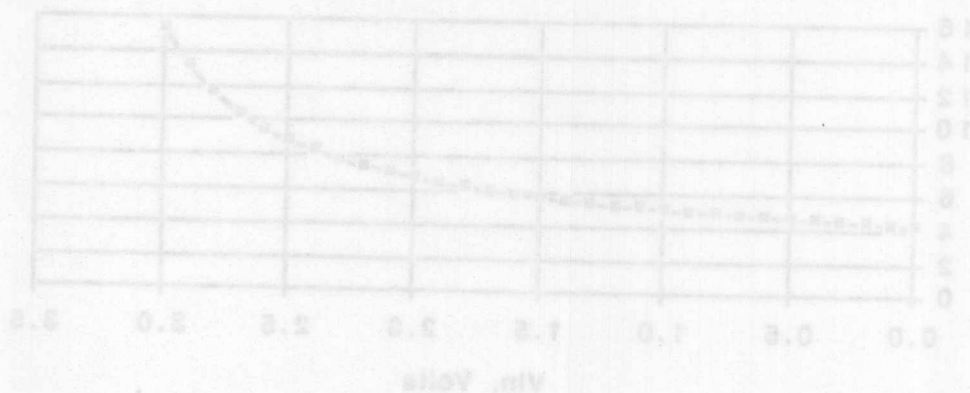
On Resistance vs Vin @ 4.75 Vcc (338X Only)



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Typ	Max	Unit
I_{cc}	Quiescent Power Supply Current	$V_{cc} = \text{MAX}, V_i = \text{GND or } V_{cc}, f = 0$	-	-	1.5	mA
ΔI_{cc}	Pwr Supply Current, per Input High (2)	$V_{cc} = \text{MAX}, \text{Input} = 3.4 \text{ V}, f = 0$ Per control input	-	-	2.5	mA
Q_{ccd}	Dynamic Pwr Supply Current per mHz (3)	$V_{cc} = \text{MAX}, \text{A \& B pins open},$ Control input toggling @ 50% duty cycle	-	-	0.25	mA/mHz
I_c	Total Power Supply Current (4,5)	$V_{cc} = \text{MAX}, \text{A \& B pins at } 0.0\text{V},$ Control inputs toggling @ 50% duty cycle $V_{ih} = 3.4\text{V}, f_{\text{clock}} = 10 \text{ mHz}$	-	-	9.0	mA

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_i = 3.4\text{V}$, control inputs only). A and B pins do not contribute to I_{cc} .
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
- $I_c = I_{\text{Quiescent}} + I_{\text{Inputs}} + I_{\text{Dynamic}}$
 $I_c = I_{cc} + \Delta I_{cc} Dh Nt + Q_{ccd} (fi Ni)$
 I_{cc} = Quiescent Current
 ΔI_{cc} = Power Supply Current for each TTL High input ($V_i = 3.4\text{V}$, control inputs only)
 Dh = Duty Cycle for each TTL input that is High (control inputs only).
 Nt = Number of TTL inputs that are at DH (control inputs only).
 fi = frequency that the inputs are toggled (control inputs only).
- Note that activity on A and/or B inputs do not contribute to I_c if A and B inputs are between gnd and V_{cc} . The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, I_c will be equal to I_{cc} only regardless of activity on the A and B pins.



SWITCHING CHARACTERISTICS OVER OPERATING RANGE (338x only)

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Note	Com		Mil		Unit
			Min	Max	Min	Max	
t PLH	Data Propagation Delay Ai to Bi, Bi to Ai	338X	2,3	0.25		0.25	ns
t PHL		358X	2,3,7	1.25		1.25	ns
t PZH	Switch Turn On Delay BEA, BEB to Ai, Bi	338X	1	1.5	1.5	7.5	ns
t PZL		358X	1,7	1.5	1.5	8.5	ns
t PLZ	Switch Turn Off Delay BEa, BEB to Ai, Bi	338X	1,2	1.5	1.5	6.5	ns
t PZL		358X	1,2,7				
Qci	Charge Injection, Typical	338X	4,6	1.5		1.5	pC
		358X	4,6,7				

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and load alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- 4) Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts.
- 5) Characterized parameter but not 100% tested.
- 6) Characterized parameter. Not 100% tested.
- 7) Preliminary data, subject to change.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (338x only)

Commercial TA = 0°C to 70°C, VCC = 5.0V±5%, MILITARY TA = -55°C to 125°C, VCC = 5.0V±10%
 Load = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes	Com		Mil		Unit
			Max	Min	Max	Min	
t _{PLH}	Data Propagation Delay	338X	2.5		0.25		ns
t _{PHL}	A1 to B1, B1 to A1	338X	2.0, 2.7		1.25		ns
t _{PLZ}	Switch Turn On Delay	338X	1	1.5	0.5	1.5	ns
t _{PZL}	BEA, BEB to A1, B1	338X	1.7	1.5	1.5	1.5	ns
t _{PLZ}	Switch Turn Off Delay	338X	1.5	1.5	0.5	1.5	ns
t _{PZL}	BEA, BEB to A1, B1	338X	1.5, 1.7	1.5	0.5	1.5	ns
t _{CO}	Charge Injection, Typical	338X	4.8		1.5		pC
		338X	4.8, 7				

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and also alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the normal times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- 4) Measured at switch turn off. A1 to C, load = 50 pF in parallel with 10 meg source impedance. Vin at A = 0.0 volts.
- 5) Characterized parameter but not 100% tested.
- 6) Characterized parameter. Not 100% tested.
- 7) Preliminary data, subject to change.



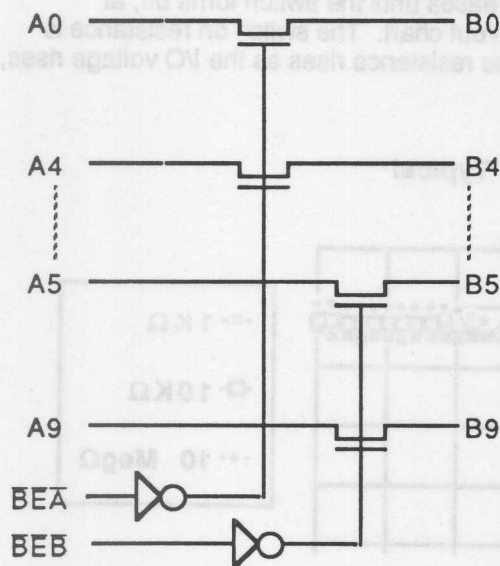
CMOS Bus Switches Provide Zero Delay Bus Communication

Application
Note
AN-09

by
David Wyland

The 74QST3383 and 74QST3384 CMOS Bus Switches by Quality Semiconductor are high speed TTL bus connect devices. When they are enabled, the bus switches directly connect two buses with a connection resistance of less than 5Ω . They are like a 5 nanosecond multi-pole relay for TTL signals with an on resistance of 5Ω . Since these devices directly connect the bus signals they introduce no additional propagation delay, timing skew or noise. They are also inherently bidirectional and dissipate no additional power. They can replace traditional TTL buffers and transceivers to reduce propagation delay, noise, control complexity and power dissipation.

A block diagram of the 74QST3384 CMOS Bus Switch is shown in Figure 1. This device consists of ten switches arranged as two banks of five. This allows the 3384 to be used as a 10-bit switch or as a 5-bit, 2-to-1 multiplexer. A block diagram of the 74QST3383 CMOS Bus Exchange Switch is shown in Figure 2. This device consists of two banks of ten switches arranged to gate through or exchange two banks of five signals. This allows the 3384 to be used as a 10-bit switch or as a 5-bit, two way bus exchange device. This part is particularly useful for exchange and routing operations such as byte swap, crossbar matrices, and RAM sharing.



PIN DESCRIPTION

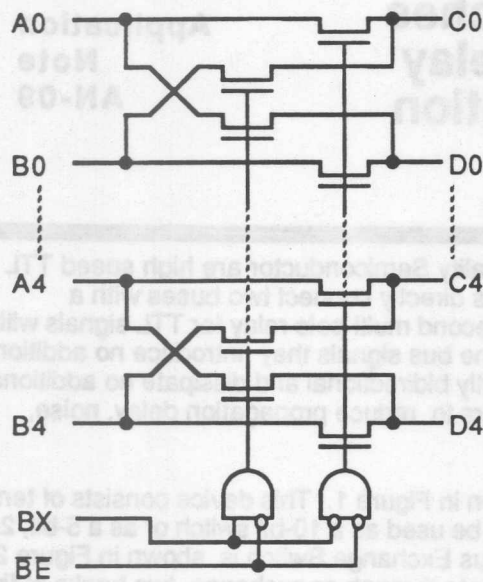
Name	I/O	Function
A0-9	I/O	Bus A
B0-9	I/O	Bus B
BEA, BEB	I	Bus Switch Enable

FUNCTION TABLE

BEA	BEB	B0-4	B5-9	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A0-4	Hi-Z	Connect
H	L	Hi-Z	A5-9	Connect
L	L	A0-4	A5-9	Connect

Figure 1: 74QST3384 CMOS Bus Switch Block Diagram

Each switch consists of an N channel MOS transistor driven by a CMOS gate. When the switch is enabled, the gate of the N channel transistor is at V_{cc} (+5 volts) and the device is on. These devices have an on resistance of less than 5Ω for voltages near ground and will drive in excess of 64 mA each. The resistance rises somewhat as the I/O voltage rises from a TTL low of 0.0 volts to a TTL high of 2.4 volts. In this region the A and B pins are solidly connected, and the bus switch is specified in the same manner as a TTL device over this range. As the I/O voltage rises to approximately 4.0 volts, the transistor turns off. This corresponds to a typical TTL high of 3.5 to 4.0 volts.



PIN DESCRIPTION

Name	I/O	Function
A0-4, B0-4	I/O	Buses A, B
C0-4, D0-4	I/O	Buses C, D
BE	I	Bus Switch Enable
BX	I	Bus Exchange

FUNCTION TABLE

BE	BX	A0-4	B0-4	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C0-4	D0-4	Connect
L	H	D0-4	C0-4	Exchange

Figure 2: 74QST3383 CMOS Bus Exchange Switch Block Diagram

The bus switch provides a low resistance connection between inputs and outputs for voltages below 3.0 volts. As the I/O voltage rises above 3 volts, the resistance increases until the switch turns off, at approximately 4.0 volts. This is shown in Chart 1, a V_{in} versus V_{out} chart. The switch on resistance is determined by the lower of the voltages on the two I/O pins. The resistance rises as the I/O voltage rises, as shown in Chart 2.

Vout vs Vin for Various Loads, Typical

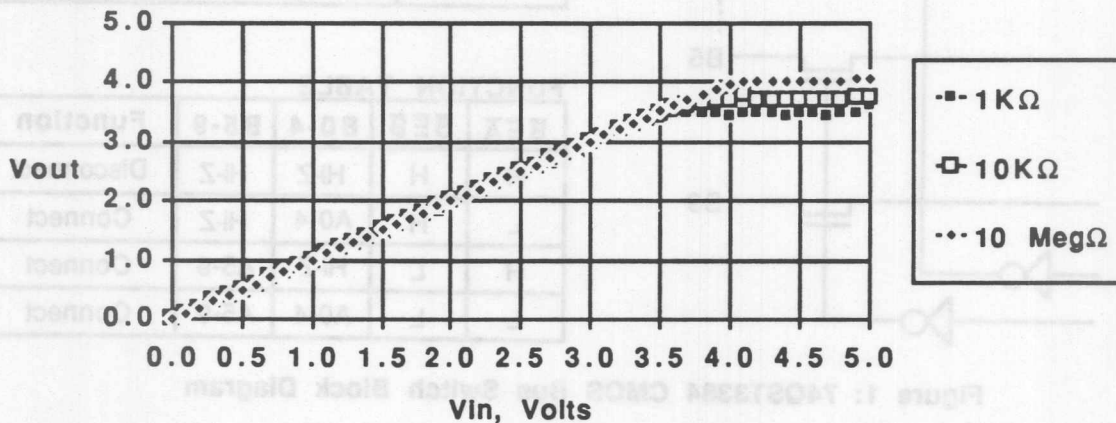
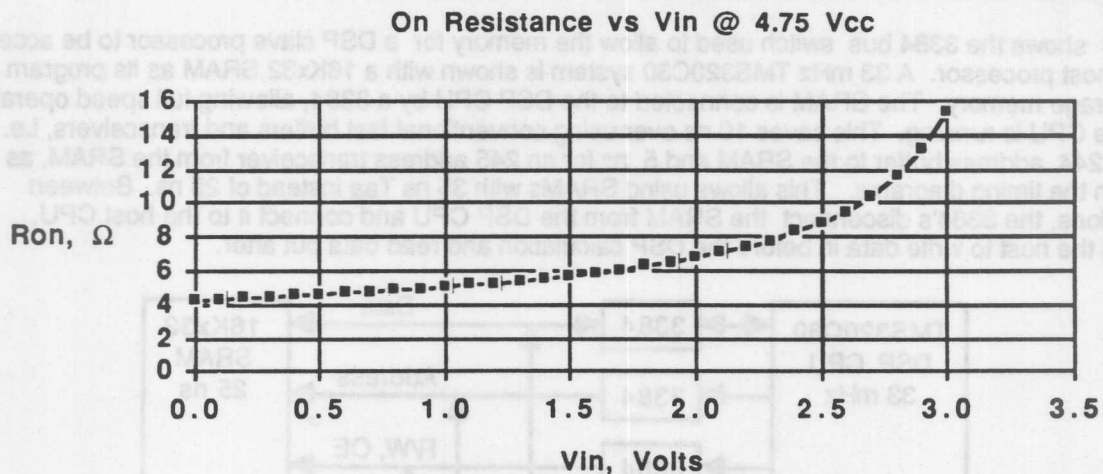


Chart 1: Vout vs Vin

Chart 2: Switch On Resistance vs V_{in}

The bus switch provides a path for a driving device to drive capacitance to ground and to drive capacitance up from ground. This is shown in Figure 3. When the A (or B) input is driven to a TTL low of 0.0 volts, the N channel transistor is fully on and the B (or A) output will follow it. Likewise, when the A (or B) input is driven from a TTL low of 0.0 volts to a TTL high, the capacitor side of the N channel switch is at 0.0 volts, the switch is fully on and the B (or A) output will follow it through threshold and beyond. This means that the rise and fall time characteristics and waveforms of the B (or A) output will be determined by the TTL driver, not the bus switch. The switch introduces no propagation delay, to a first approximation.

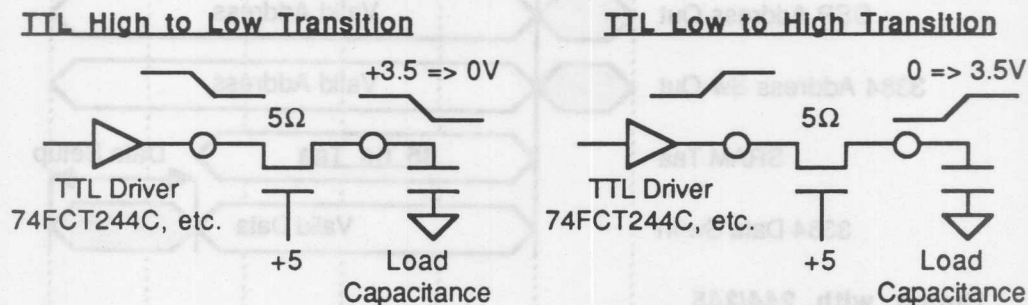


Figure 3: CMOS Bus Switch Operation

When the bus switch is disabled, the N channel transistor gate is at 0.0 volts, and the transistor is off. By the nature of the N Channel transistor design, the A and B pins are fully isolated when the transistor is off. Leakage and capacitance is to the chip substrate (i.e., ground) rather than between input and output. This minimizes feedthrough in the off state. Because only an N channel transistor is used, either A or B pin(s) can be taken to V_{cc} and above, and the device can be powered down without loading either bus.

The bus switch can replace drivers and transceivers in systems if bus repowering is not required. Since the bus switch directly connects two buses, it provides no drive of its own but relies on the device that is driving data onto the connected buses. If the additional loading of the connected bus is small enough, there is a net gain in speed. For example, the sensitivity to loading of a driver such as the 74FCT244 is typically 2 ns/100 pF. If the connected bus adds 50 pF of loading the added delay will be 1 ns. This is much less than the 4 to 10 ns delay of the buffer or transceiver the bus switch replaces.

Microprocessor Shared Memory Connect for Slave Processor

Figure 4 shows the 3384 bus switch used to allow the memory for a DSP slave processor to be accessed by the host processor. A 33 mHz TMS320C30 system is shown with a 16Kx32 SRAM as its program and data storage memory. The SRAM is connected to the DSP CPU by a 3384, allowing full speed operation while the CPU is running. This saves 10 ns over using conventional fast buffers and transceivers, i.e. 5 ns for a 244 address buffer to the SRAM and 5 ns for an 245 address transceiver from the SRAM, as shown in the timing diagrams. This allows using SRAMs with 35 ns Taa instead of 25 ns. Between calculations, the 3384's disconnect the SRAM from the DSP CPU and connect it to the host CPU, allowing the host to write data in before the DSP calculation and read data out after.

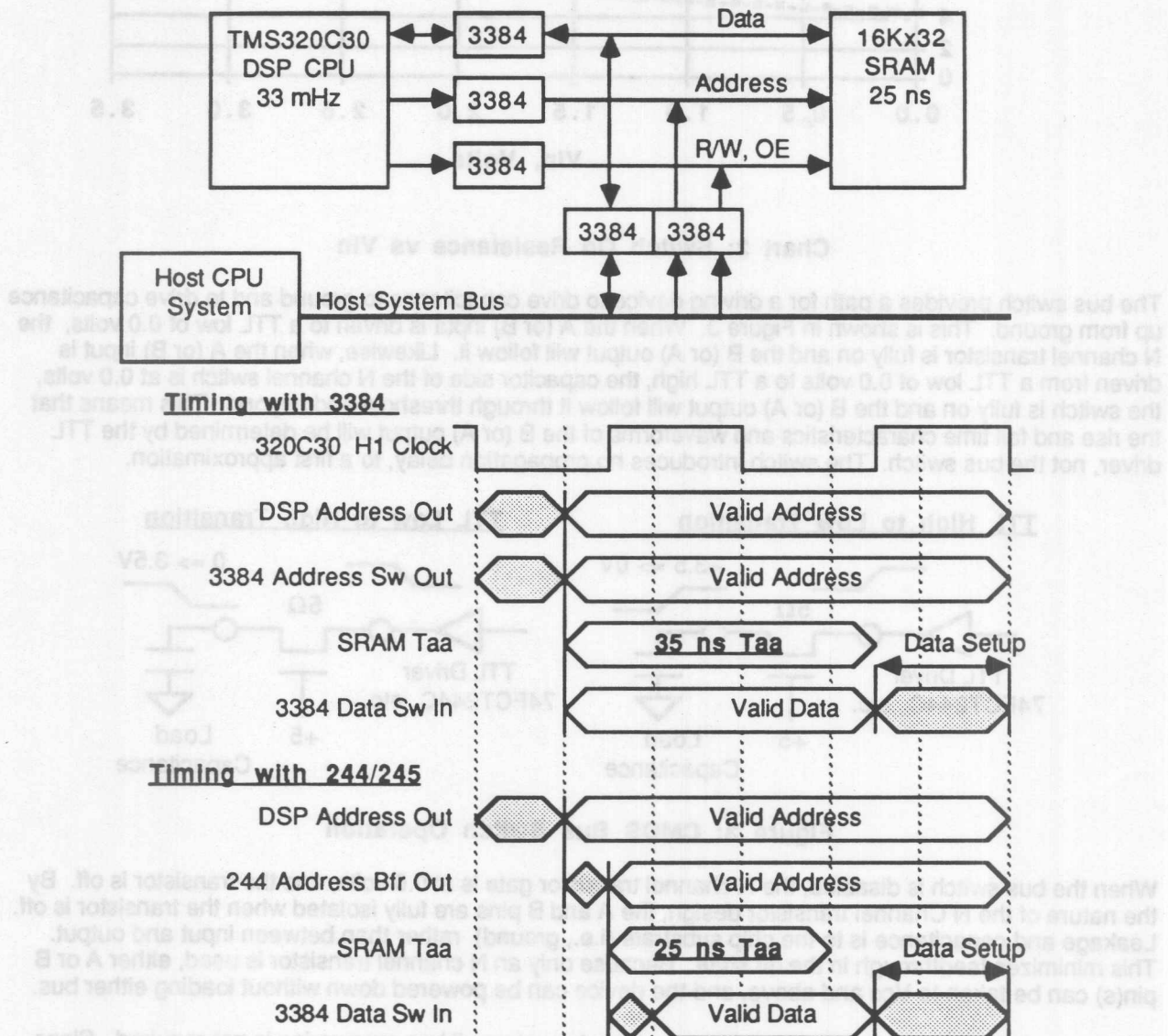


Figure 4: 74QST3384 as DSP Shared Memory Connect

Multiprocessor System Fast Bus Connect

Figure 5 shows the 3384 bus switch used as a fast bus connect in a high performance multiprocessor system. Four 32-bit processors are shown, each with its own cache or other local memory. Each processor is connected by a 3384 bus switch to a 1 meg x 32, 25 ns cycle time fast SRAM main memory. The 3384 is used to connect the address, data, and control lines of the SRAM directly to each processor. When one of the 3384's is active, the main memory appears as a simple SRAM to the connected CPU. This provides a simple, very fast interface with no additional delays for buffers or data direction logic and no timing skew in the control signals.

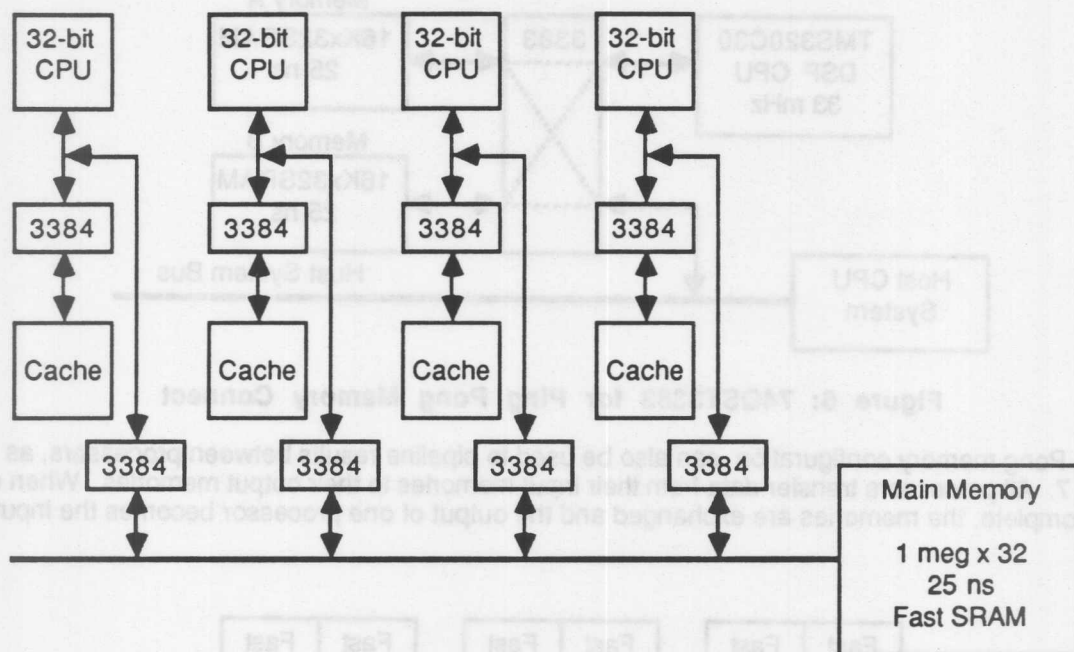


Figure 5: 74QST3384 as Multiprocessor System Bus Connect

Bus Exchange Switch for Ping Pong Memory Connect

Figure 6 shows the 3383 bus exchange switch used to connect two memories to a DSP processor and a host CPU bus. The 3383 connects Memory A to either the DSP or host CPU, and Memory B to the host CPU or DSP CPU, respectively, depending on the state of the bus exchange control. This configuration allows the host CPU to be accessing one memory for loading program and data or retrieving results while the DSP CPU is running out of the other memory. When the calculation is complete, the memories are exchanged, and the DSP CPU can continue with another calculation while the results of the last one are accessed. This configuration allows both high speed and high throughput.

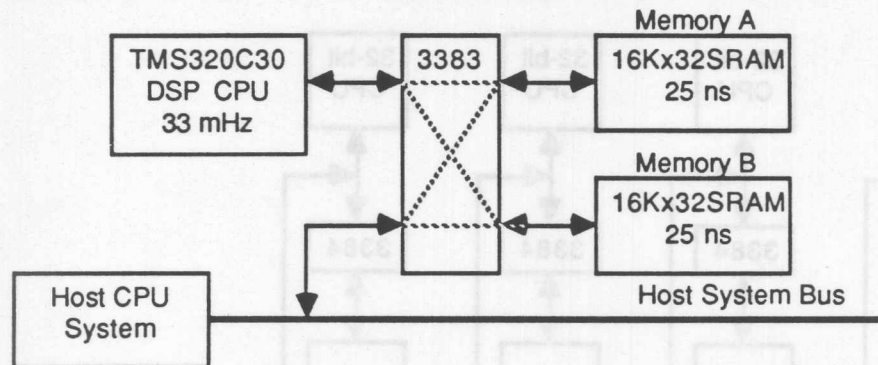


Figure 6: 74QST3383 for Ping Pong Memory Connect

The Ping Pong memory configuration can also be used to pipeline results between processors, as shown in Figure 7. All processors transfer data from their input memories to their output memories. When one pass is complete, the memories are exchanged and the output of one processor becomes the input of the next.

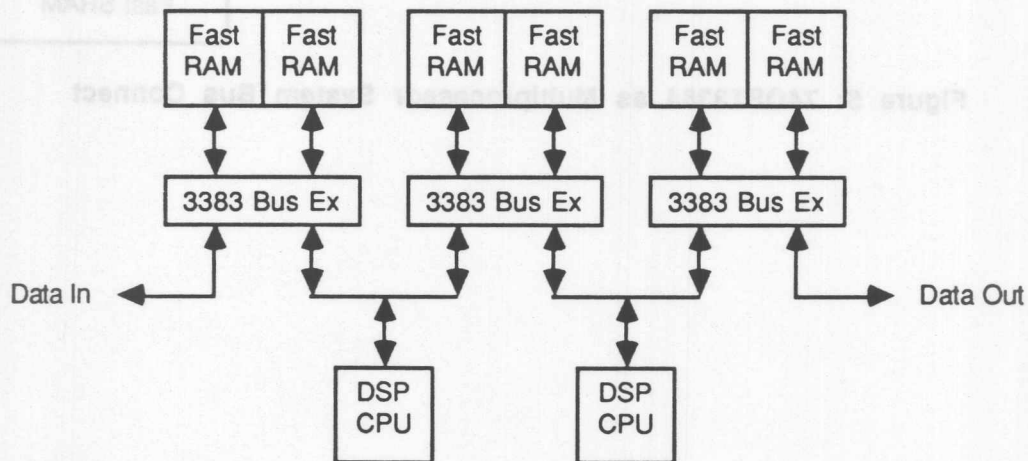


Figure 7: 74QST3383 for Ping Pong Pipeline Memory

Bus Exchange Switch for Crossbar Systems

Figure 8 shows the 3383 bus exchange switch used to connect four CPUs and four memories in a crossbar configuration. In this configuration, any CPU can be connected to any memory. If there is no conflict by two CPUs for the same memory, any valid combinations of CPU and memory can be made by appropriate selection of the 3383 controls. Two layers of 3383 bus exchange switches are required for this four-way crossbar. Three layers will be required for an 8-way crossbar, etc.

The 3383 bus exchange switch is ideal for crossbar work because it introduces no delay of its own. A 16-way crossbar with four layers of switches adds little or no delay over direct connection of the RAM to the CPU. Also, the CPU sees a simple RAM interface without the complicated timing skew requirements which might be imposed by using bus transceivers instead of 3383 switches.

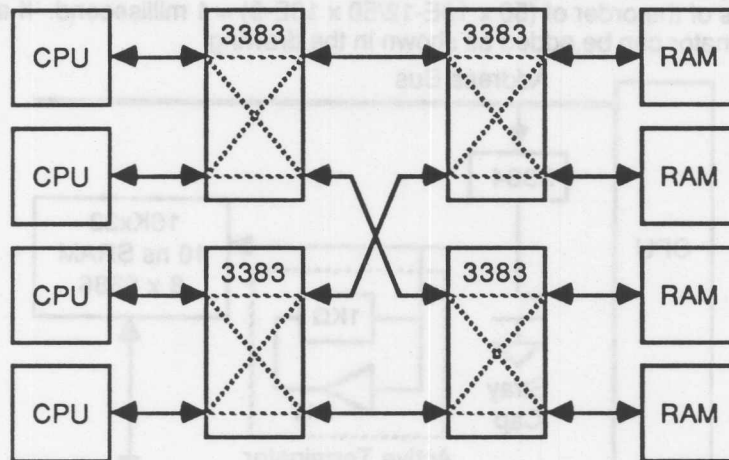


Figure 8: 74QST3383 Crossbar Switch

Bus Exchange Switch for Bus Byte Swap and Barrel Shift

A scheme similar to the one shown in the diagram of Figure 8 can also be used to provide byte swap capability between a CPU and memory. This is useful in systems where big-endian and little-endian byte orders are mixed within the same system. If the CPU and RAM blocks of figure 8 are interpreted as bytes of a CPU and memory bus respectively, the crossbar switch scheme shown allows any combination of byte swapping or shifting desired without introducing any additional propagation delay or control considerations. If this concept is extended to the bit level, a barrel shifter results.

Fast Address Latch

Figure 9 shows the 3384 bus switch used as a fast address latch in an SRAM memory subsystem. In this system, the 3384 connects the SRAM to the address bus, which drives the stray capacitance of the SRAM array. When the 3384 turns off, the stray capacitance holds the TTL level. The advantage of using the 3384 instead of a fast latch such as the 74FCT373 is that the effective throughput delay is much less. The delay caused by the additional 50 pF load on the address bus may be 1 ns as compared to 4 ns for the fastest latch. Also, the 3384 does not introduce additional noise.

The hold time for typical capacitances and leakages can be quite long compared to the clock cycle times of fast systems. For the 16Kx32 configuration of eight 16Kx4 SRAMs shown, the stray capacitance is of the order of 50 pF. The turn off transient of the 3384 will typically be less than 50 millivolts. Assuming a 1 volt change in level and a typical total leakage at operating temperature of less than 50 nanoamperes, (SRAMs + 3384), the hold time is of the order of $(50 \times 10^{-12} / 50 \times 10^{-9}) = 1$ millisecond. If an indefinite hold is desired, an active terminator can be added as shown in the drawing.

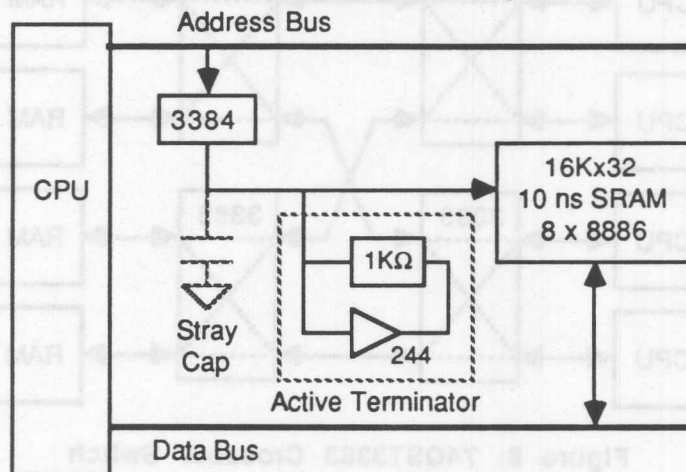


Figure 9: 74QST3384 Fast Address Latch

ATE Load Switch

Figure 10 shows the 3384 bus switch used as a load switch for an automated test equipment (ATE) load board. ATE equipment requires custom design of the load board (i.e. electrical test fixture) for a given device to be tested. A common problem to be solved is the connection and disconnection of load resistor network to each pin of the device under test (DUT). The load must be connected during parts of the test and disconnected during other parts. This connection is typically done with small relays because of their low on resistance. However, relays are large and slow. The 3384 bus switch can replace up to 10 relays in this application, in a smaller package, and with an actuation time of 6 nanoseconds rather than 5 milliseconds. This can significantly speed up test time.

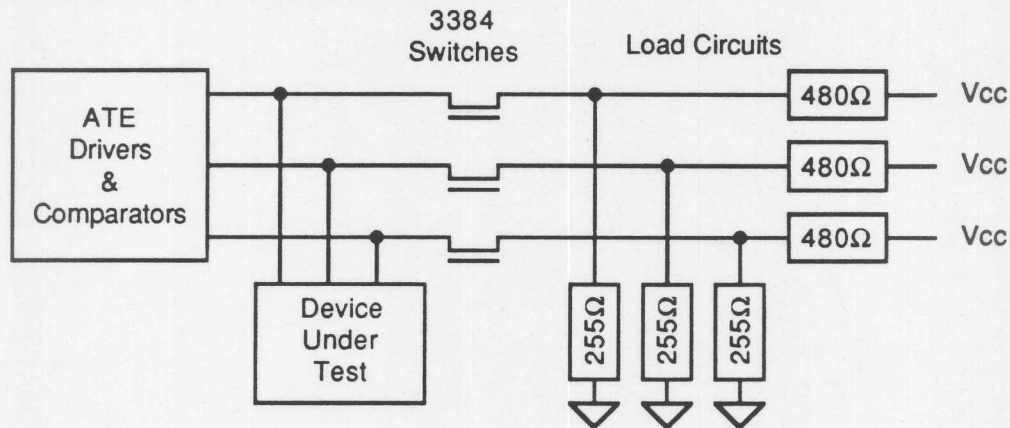


Figure 10: 74QST3384 ATE Load Switch

Conclusion

The 74QST3383 and 3384 bus switches are new tools for the system designer. They can be used to reduce propagation delay and to create high speed systems with simplified interfaces, improved timing margins and reduced noise.

ATE Load Switch

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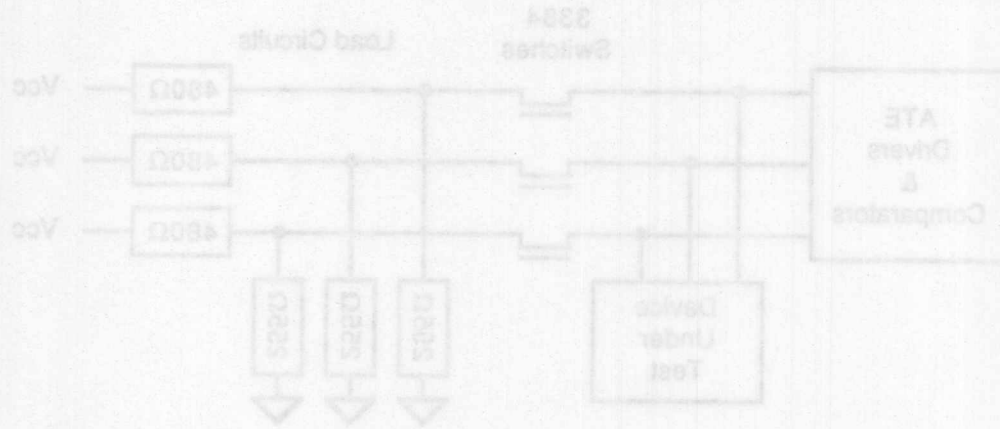


Figure 10: 3384 ATE Load Switch

Conclusion

The 740ST3383 and 3384 bus switches are new tools for the system designer. They can be used to reduce propagation delay and to create high speed systems with simplified interconnects, improved timing margins and reduced noise.

Q

Bus Switches Provide 5 Volt to 3 Volt Logic Conversion with Zero Delay

Application
Note
AN-11

by
David Wyland

Abstract

Battery operated computer systems, such as notebook computers, need support logic with a combination of high speed and low power. High speed logic is required to support high speed microprocessors. Low power is required to maximize battery life. Three volt TTL (3V TTL) logic families have been introduced to supply these needs. The 3V TTL logic families have the same TTL I/O specifications as their 5 Volt relatives (5V TTL) but with a 3.3 Volt Vcc instead of 5 Volt. Many systems have a mixture of 5V TTL and 3V TTL logic, and conversion between the two types is required to prevent damage to the 3V TTL even though their logic levels are compatible. The 74QST3384 QuickSwitch™ bus switches can be used to provide this conversion automatically without requiring control logic or introducing propagation delay.

Background

A common problem in low power system design is a requirement for a mixture of 5 Volt and 3 Volt logic because some functions are not yet available in 3 Volt form. An example of such a system is shown in Figure 1. The CPU and DRAM use 3.3 Volt Vcc, while the EPROM and I/O devices use 5 Volt Vcc.

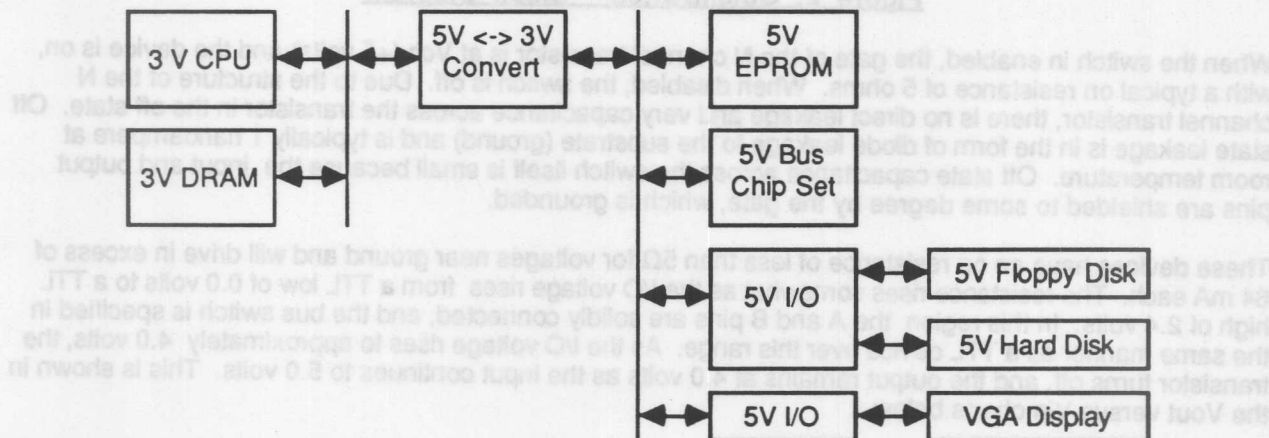


Figure 1: 5 Volt & 3 Volt Logic Mixture In PC Design

A 5 Volt to 3 Volt converter is shown in Figure 1 because the 5V TTL cannot, in general, drive the 3V TTL even though their logic levels are compatible. A 5V TTL CMOS driver will drive the bus to 5 Volts at a logic high. Even low voltage swing TTL devices such as the FCTT family have TTL high output voltages above 4.0 volts. The 3V TTL CMOS devices cannot withstand more than approximately 3.3 Volts on their I/O pins. If an I/O pin of a 3V TTL CMOS device is driven above its 3.3 Volt Vcc, the P Channel device in the output driver will conduct causing current flow from the bus to the 3.3 Volt Vcc through the device. The resulting high current flow can cause destruction of the 3V TTL device output through latchup effects. The function of the 5 Volt to 3 Volt converter is to limit the voltage seen by the 3V TTL device to acceptable levels, typically no more than the 3.3 Volt Vcc + 0.5 volts.

A 5V TTL to 3V TTL converter could consist of specialized buffers and transceivers which would accept 5V TTL levels on one side and 3V TTL levels on the other. These parts would add propagation delay to the signal path, and would require data direction control in the case of bidirectional buses.

Fortunately, a simpler 5V TTL to 3V TTL converter exists: the QuickSwitch™ bus switch. These devices can be used to provide bidirectional 5V TTL to 3V TTL conversion with no added propagation delay or direction control. Under the appropriate conditions, the QuickSwitch™ will accept 5V TTL signals on the driving side while limiting the voltage output to 3.3 Volts for 3V TTL on the driven side. Also, the QuickSwitch™ is equivalent to a 5Ω resistor when on so that it adds no significant propagation delay to signals passing through it. To understand this, we will examine the QuickSwitch™ and its operation.

The QuickSwitch™ CMOS Bus Switch

The basic element of the QuickSwitch™ is a fast, low on resistance, low capacitance, high current capacity switch. The combination of low on resistance and low capacitance is provided by the QCMOS™ short channel length, high performance CMOS process. Each switch consists of an N channel MOS transistor driven by a CMOS gate, as shown below.

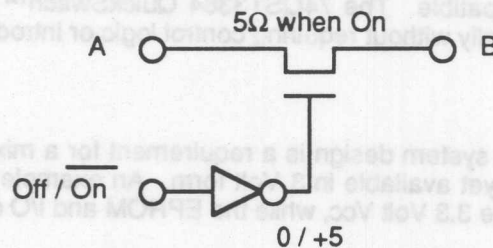


Figure 2: QuickSwitch™ Block Diagram

When the switch is enabled, the gate of the N channel transistor is at Vcc (+5 volts) and the device is on, with a typical on resistance of 5 ohms. When disabled, the switch is off. Due to the structure of the N channel transistor, there is no direct leakage and very capacitance across the transistor in the off state. Off state leakage is in the form of diode leakage to the substrate (ground) and is typically 1 nanoampere at room temperature. Off state capacitance across the switch itself is small because the input and output pins are shielded to some degree by the gate, which is grounded.

These devices have an on resistance of less than 5Ω for voltages near ground and will drive in excess of 64 mA each. The resistance rises somewhat as the I/O voltage rises from a TTL low of 0.0 volts to a TTL high of 2.4 volts. In this region the A and B pins are solidly connected, and the bus switch is specified in the same manner as a TTL device over this range. As the I/O voltage rises to approximately 4.0 volts, the transistor turns off, and the output remains at 4.0 volts as the input continues to 5.0 volts. This is shown in the Vout versus Vin charts below.

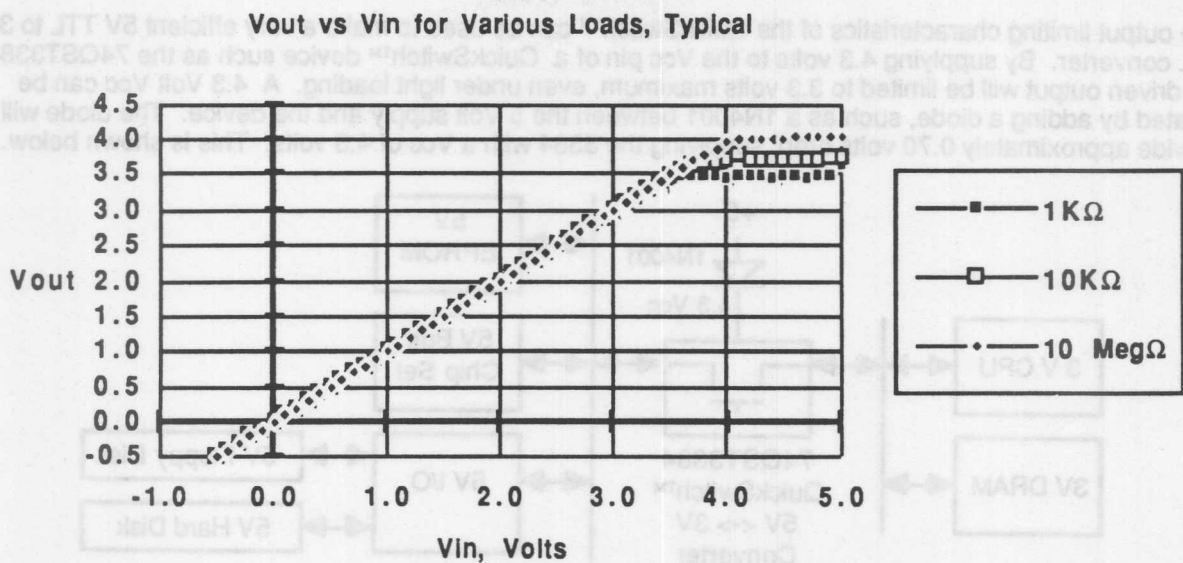


Figure 3: QuickSwitch™ Vout vs Vin

QuickSwitch™ Vout versus Vcc

The QuickSwitch™ output voltage for an input voltage equal to Vcc is approximately 1.0 volt below Vcc. This voltage drop varies from 1.0 volts at light loading (μA) to 1.5 volts at heavier loading (mA). Increasing or decreasing Vcc will increase or decrease the output voltage by the same amount, as shown in the plot below. In this plot, the " ΔV " curves shown the difference between the output and Vcc, i.e. the voltage drop across the switch. The output limit of 1.0 volt below Vcc is because an N channel transistor is used as the switch which turns off as its gate to source voltage falls below this value.

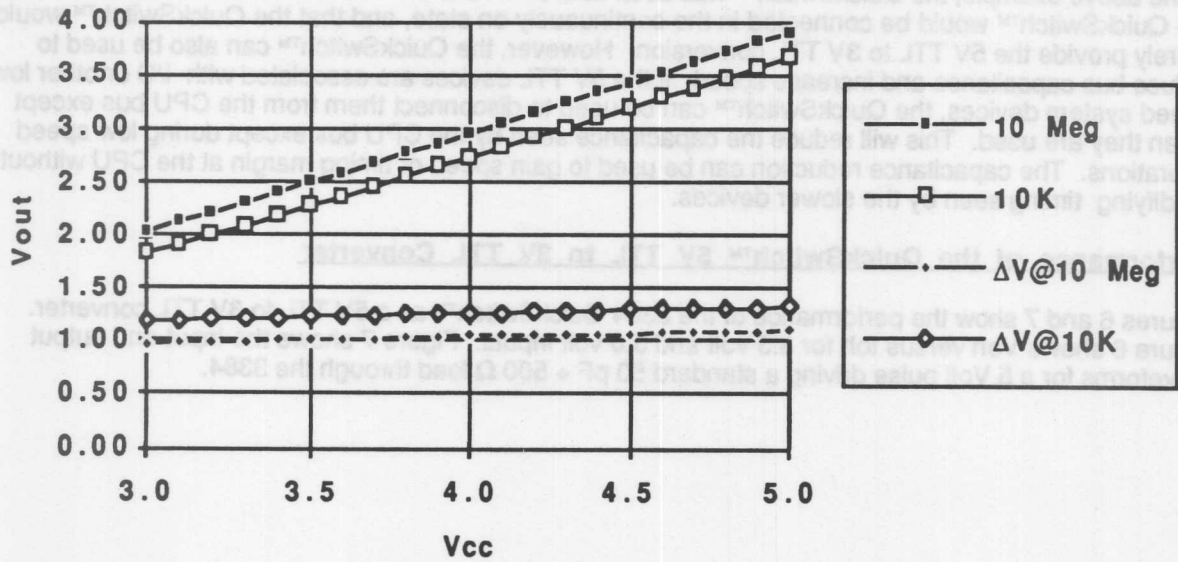


Figure 4: QuickSwitch™ Vout and Voltage Drop versus Vcc at Vin = Vcc

QuickSwitch™ As A 5V TTL to 3V TTL Converter

The output limiting characteristics of the QuickSwitch™ can be used to make a very efficient 5V TTL to 3V TTL converter. By supplying 4.3 volts to the Vcc pin of a QuickSwitch™ device such as the 74QST3384, the driven output will be limited to 3.3 volts maximum, even under light loading. A 4.3 Volt Vcc can be created by adding a diode, such as a 1N4001 between the 5 Volt supply and the device. The diode will provide approximately 0.70 volts drop, supplying the 3384 with a Vcc of 4.3 volts. This is shown below.

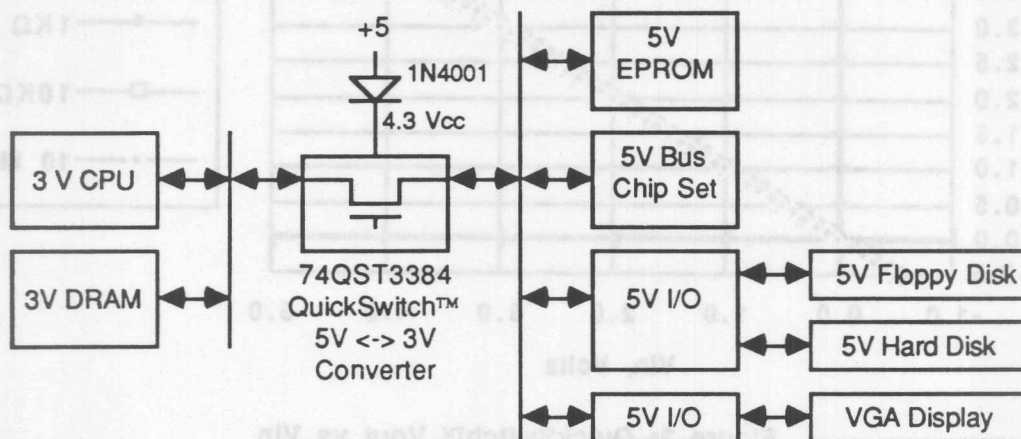


Figure 5: System with QST3384 as 5V TTL to 3V TTL Converter

The 74QST3384 devices provide 10 bits of conversion per device. A bus with a 24-bit address bus, a 16-bit data bus, and up to 10 control lines would require 5 devices. Note that the conversion is bidirectional and automatic. If either side is driven to 5 Volts, the driven side will be limited to 3.3 volts.

Using QuickSwitch™ to Improve Speed by Reducing Capacitance

In the above example, the QuickSwitch™ was used as a 5V TTL to 3V TTL Converter. It was assumed that the QuickSwitch™ would be connected in the continuously on state, and that the QuickSwitch™ would merely provide the 5V TTL to 3V TTL conversion. However, the QuickSwitch™ can also be used to reduce bus capacitance and increase speed. If the 5V TTL devices are associated with I/O or other low speed system devices, the QuickSwitch™ can be used to disconnect them from the CPU bus except when they are used. This will reduce the capacitance seen by the CPU bus except during low speed operations. The capacitance reduction can be used to gain speed or timing margin at the CPU without modifying timing seen by the slower devices.

Performance of the QuickSwitch™ 5V TTL to 3V TTL Converter

Figures 6 and 7 show the performance of the 3384 QuickSwitch™ as a 5V TTL to 3V TTL converter. Figure 6 shows Voh versus loh for 3.3 volt and 5.0 volt inputs. Figure 7 shows the input and output waveforms for a 5 Volt pulse driving a standard 50 pF + 500 Ω load through the 3384.

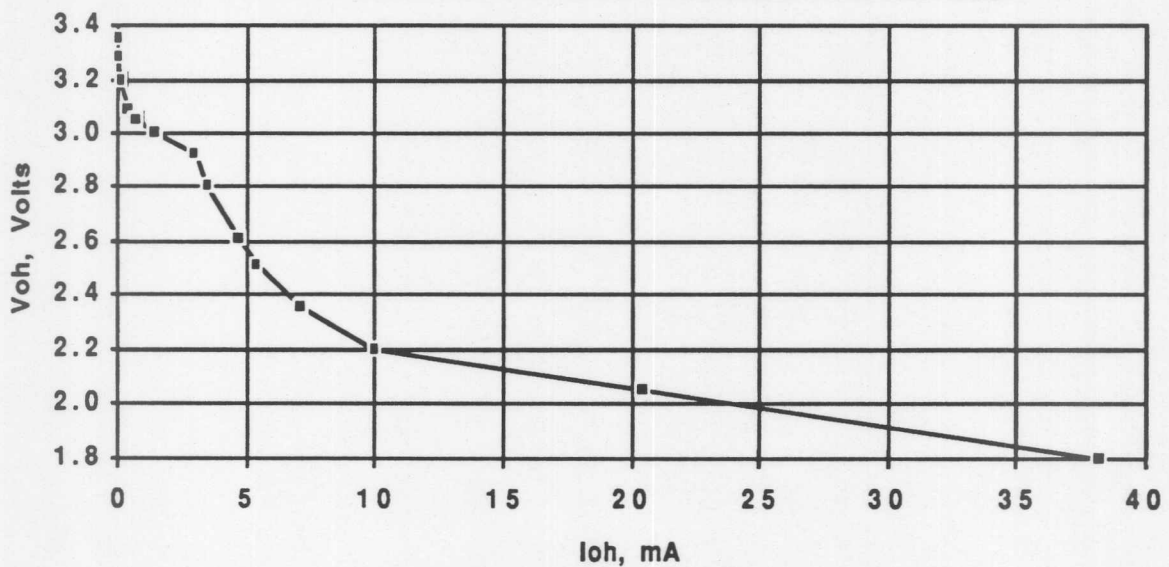
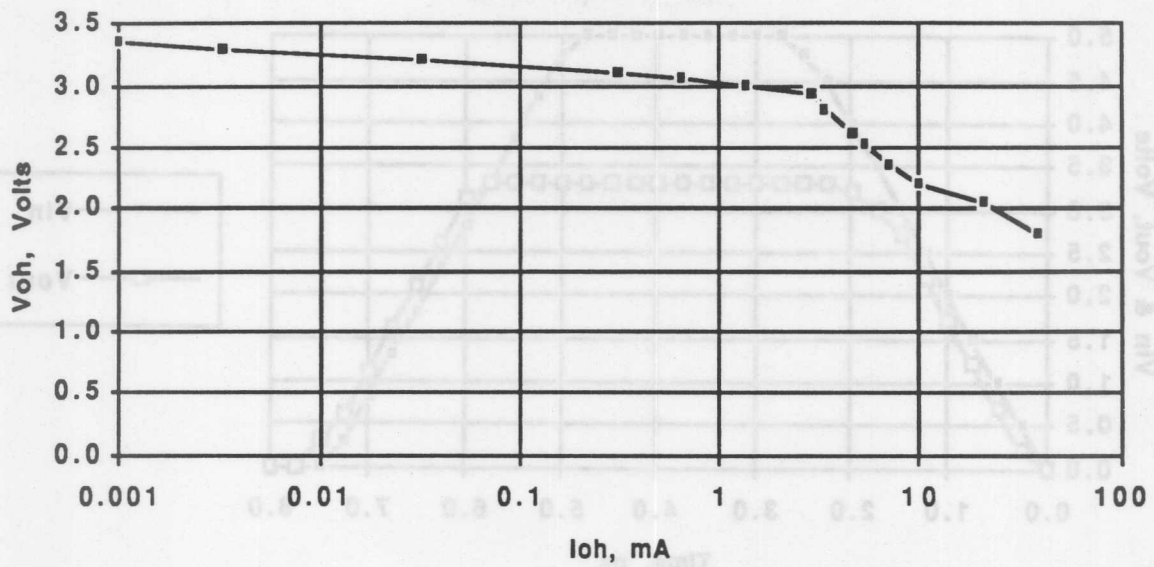


Figure 6: Voh vs Ioh for QST3384 with Vcc = 4.3 Volts & Vin = 3.3 & 5.0 Volts

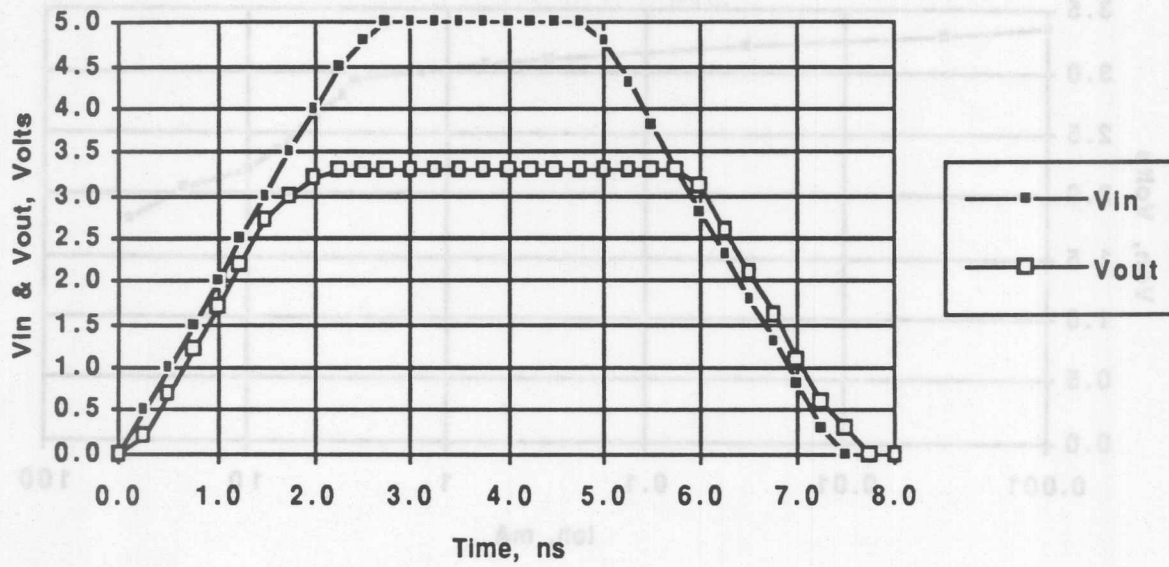


Figure 7: Input to Output Delay of QST3384 at Vcc = 4.3 Volts

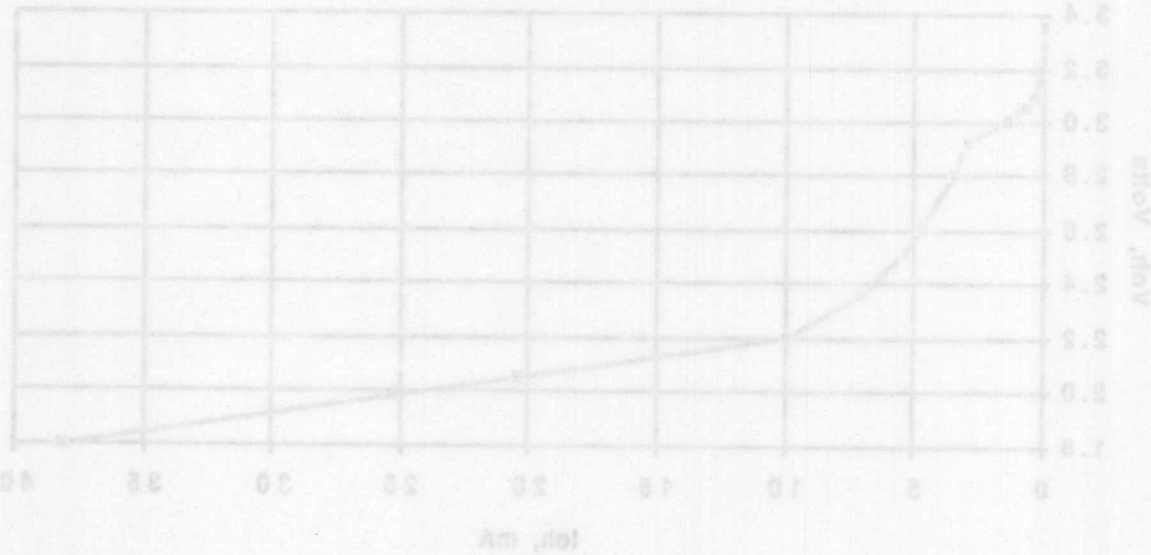


Figure 8: Voh vs Ioh for QST3384 with Vcc = 4.3 Volts & Vin = 5.0 Volts

Q

Use QuickSwitch™ Bus Switches to Make Large, Fast Dual Port RAMs

Application
Note
AN-12

by
David Wyland

Abstract

Dual port RAMs are effective devices for high speed communication between microprocessors. Typical dual port RAMs are specialty SRAMs of small size (1K to 4K bytes) and medium speed (25-50 ns). Because of their relatively low density, it is usually impractical in terms of chip count and cost to make large dual port RAM systems from these chips. There is another approach to making dual port RAMs, however. QuickSwitch™ bus switches can be combined with standard high speed SRAMs to make large, fast time shared dual port RAMs and high performance ping pong RAM systems at low chip count and low cost.

Background

A dual port RAM is a single RAM, typically an SRAM, which can be accessed simultaneously from two different ports, one port per microprocessor. Each microprocessor sees a simple SRAM interface, and the contents of the SRAM are common to both microprocessors. A block diagram of a dual port RAM in a dual microprocessor system is shown below. In this case, a conventional CPU communicates with a DSP CPU through the common memory of the dual port RAM.

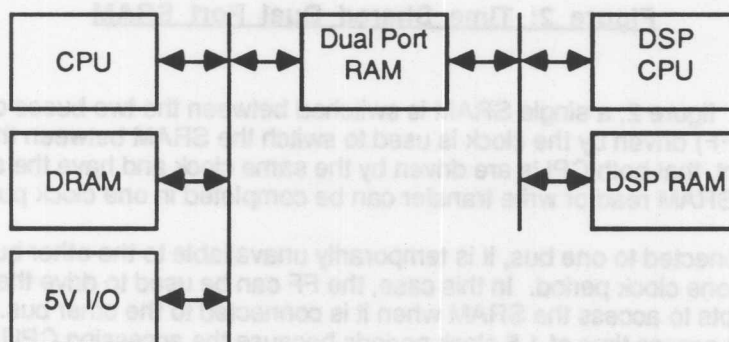


Figure 1: Dual Port RAM In Dual Microprocessor System

A true dual port RAM has one set of SRAM cells and two independent sets of addressing logic, called ports. The RAM cells may be read or written by either side independently and simultaneously. This capability is valuable because each port may access the RAM cells without regard to activities on the other port. There is one exception to this simultaneous access. If one port is writing to a cell while the other port is reading the same cell, the data may be changing during the read which could cause errors. Most dual port RAMs provide address contention logic to prevent this unlikely condition by causing one side to wait if both are trying to access the same cell.

True dual port RAMs have some limitations. The dual port RAM cell is approximately twice as large as its single port SRAM counterpart. This makes true dual port RAMs more expensive than SRAMs. They are also currently available only in lower densities, typically 1Kx8 through 4Kx8, at medium speeds, 25 to 55 ns Taa, and in large packages of 48 or more pins. For these reasons, it is generally impractical to make large, fast dual port RAM systems using these chips. However, there is more than one way to achieve the dual port RAM function.

Time Shared Dual Port SRAM

The dual port RAM function requires that each port have a simple SRAM interface and its access be independent of activity on the other port, to a first approximation. If the system timing for both ports is related or synchronized such as by being generated from the same clock, a dual port RAM function can be created by time sharing a single SRAM. This approach uses conventional SRAMs which combine high density, high speed and low cost. A block diagram of this approach is shown in Figure 2.

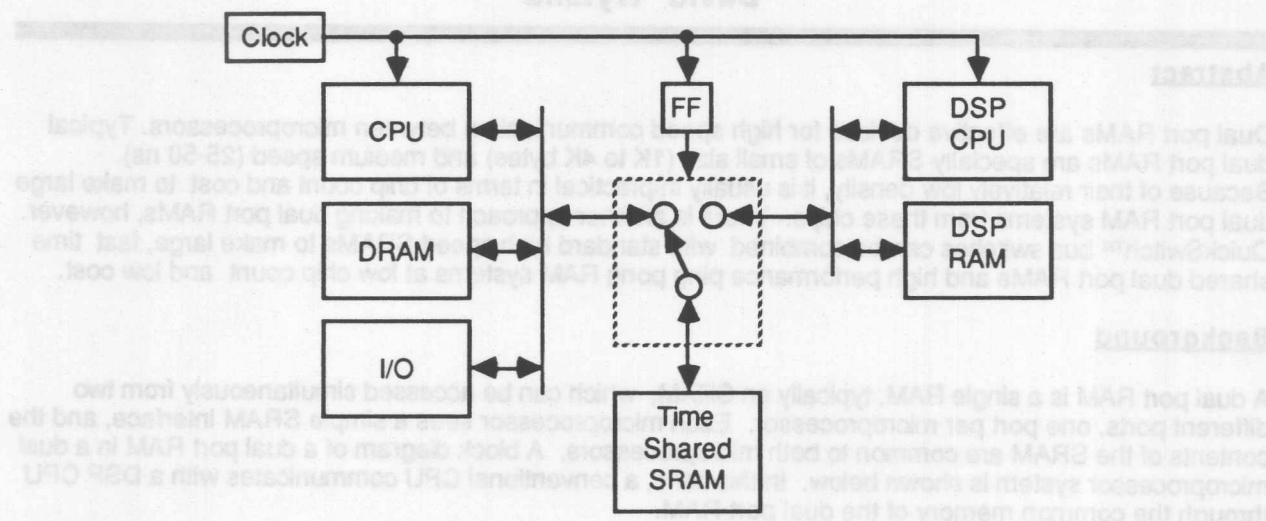


Figure 2: Time Shared Dual Port SRAM

In the system shown in figure 2, a single SRAM is switched between the two buses of the CPU and the DSP CPU. A flip flop (FF) driven by the clock is used to switch the SRAM between the buses. Let us assume, for the moment, that both CPUs are driven by the same clock and have the same bus transfer conditions, i.e. that an SRAM read or write transfer can be completed in one clock pulse.

When the SRAM is connected to one bus, it is temporarily unavailable to the other bus. However, this condition lasts for only one clock period. In this case, the FF can be used to drive the WAIT input of each CPU if that CPU attempts to access the SRAM when it is connected to the other bus. This means that the dual port SRAM has an access time of 1.5 clock periods because the accessing CPU will have to wait one clock period 50% of the time. More sophisticated logic and timing could eliminate this 0.5 clock period wait state in most cases, if necessary.

There are several advantages to the time shared dual port SRAM. Conventional SRAMs can be used, allowing high density and speed at low cost. Since one switch is used, the SRAM subsystem can be of arbitrary size; a big dual port SRAM is as easy to make as a small one. Finally, there is no contention between the two ports. Contention occurs in true dual port SRAMs when the same cell is being simultaneously written by one port and read by the other port. In this case, data will be changing during the read. This does not occur in time shared dual port SRAMs because the time shared SRAM is connected to only one port at a time. The write operation occurs at a separate time from the read, and the read data cannot change during the read.

Time Shared Dual Port SRAM Timing

A block diagram of a time shared dual port SRAM using 74QST3383 QuickSwitch™ bus switches for the switching element is shown in Figure 3. The 3383 devices are being used as 2:1 multiplexers. Each 3383 controls 5 signals. A 64Kx16 SRAM with 16 address, 16 data, one WE and one OE line have $(16+16+1+1) = 34$ signals and require seven 3384 devices.

A timing diagram of this design is shown in Figure 4. Shown in the timing diagram is a read cycle on bus A followed by a write cycle on bus B. The effective access time of the SRAM for the read cycle is the bus switch time plus the SRAM Taa. The switch time is the sum of the FF settling time and the 3383 switch time. For a FF such as the 74FCT374C with a clock to output delay of 5.2 ns and a 3383 with a switch time of 6.5 ns, the total switch time is $5.2 + 6.5 = 11.7$ ns. If a 10 ns Taa SRAM is used, this results in an effective Taa of 21.7 ns. The cycle time for the write cycle is the same, with both address and write data being delayed by the 3383 QuickSwitch™ switching time. Thus, it is reasonable to construct a time shared SRAM with a 25 ns half cycle time, allowing operation on 40 MHz buses. If the delay through the FF can be compensated for, 20 ns half cycle times may be possible, corresponding to 50 MHz buses.

Note that the SRAM Write Enable (WE) input must be high on both ports when the buses are being switched. Since this occurs at the beginning of the cycle when the WE signal on both buses is high (assuming the same bus timing), the 3383 output will remain high when switching between them.

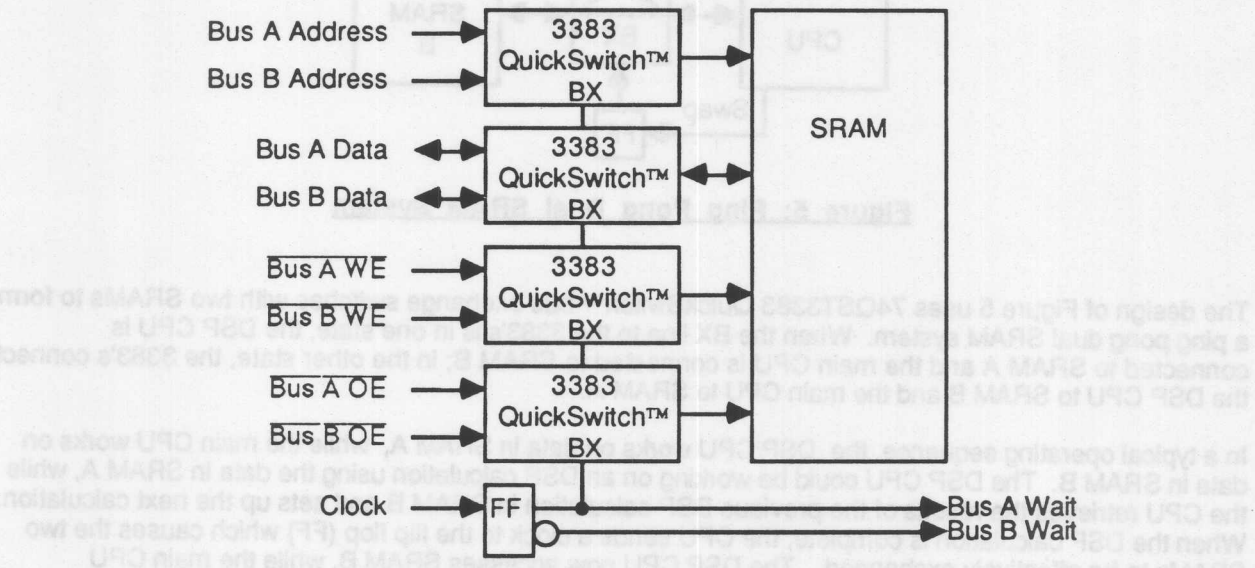


Figure 3: Time Shared Dual Port SRAM using QuickSwitch™

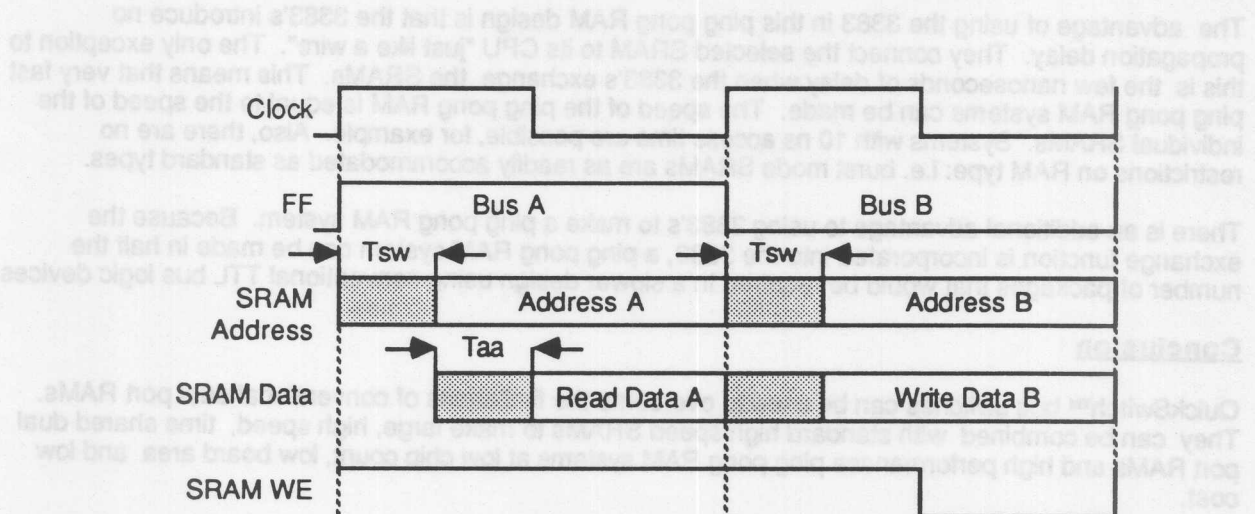


Figure 4: Time Shared Dual Port SRAM Timing Diagram

Ping Pong Dual SRAM

The highest performance dual port RAM architecture is the ping pong RAM shown in Figure 5. The ping pong RAM provides the ability to exchange blocks of data between processors rather than individual words. In the ping pong RAM, two RAMs are used, one for each processor. Each processor performs data on the contents of its RAM. When computation is complete, the two RAMs are exchanged. This approach allows a dual port function with performance equal to that of the individual SRAMs.

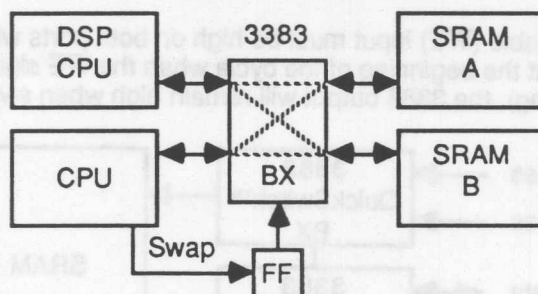


Figure 5: Ping Pong Dual SRAM System

The design of Figure 5 uses 74QST3383 QuickSwitch™ bus exchange switches with two SRAMs to form a ping pong dual SRAM system. When the BX line to the 3383's is in one state, the DSP CPU is connected to SRAM A and the main CPU is connected to SRAM B; in the other state, the 3383's connect the DSP CPU to SRAM B and the main CPU to SRAM A.

In a typical operating sequence, the DSP CPU works on data in SRAM A, while the main CPU works on data in SRAM B. The DSP CPU could be working on an DSP calculation using the data in SRAM A, while the CPU retrieves the results of the previous DSP calculation in SRAM B and sets up the next calculation. When the DSP calculation is complete, the CPU sends a clock to the flip flop (FF) which causes the two SRAMs to be effectively exchanged. The DSP CPU now accesses SRAM B, while the main CPU accesses SRAM A.

The advantage of using the 3383 in this ping pong RAM design is that the 3383's introduce no propagation delay. They connect the selected SRAM to its CPU "just like a wire". The only exception to this is the few nanoseconds of delay when the 3383's exchange the SRAMs. This means that very fast ping pong RAM systems can be made. The speed of the ping pong RAM is equal to the speed of the individual SRAMs. Systems with 10 ns access time are possible, for example. Also, there are no restrictions on RAM type: i.e. burst mode SRAMs are as readily accommodated as standard types.

There is an additional advantage to using 3383's to make a ping pong RAM system. Because the exchange function is incorporated into the 3383, a ping pong RAM system can be made in half the number of packages that would be required in a slower design using conventional TTL bus logic devices.

Conclusion

QuickSwitch™ bus switches can be used to overcome the limitations of conventional dual port RAMs. They can be combined with standard high speed SRAMs to make large, high speed, time shared dual port RAMs and high performance ping pong RAM systems at low chip count, low board area and low cost.

Q

QuickSwitch™ Converts TTL Logic to Hot Plug Operation

Application
Note
AN-13

by
David Wyland

Abstract

QuickSwitch™ bus switch devices can be used to convert TTL logic to "hot plug" operation. Hot plug means the ability to replace a card in a system without powering down the system. This is a requirement in zero downtime, 24 hour operation systems such as systems for transaction processing (airline reservations, etc.), manufacturing control, communication (telephone) and power plant control. Hot plug operation has special requirements. When the card is plugged in, it must not disturb the operation of the system even though the card initially has no power applied to it. Some families of TTL logic, such as QSI's 74FCTT logic, provide this capability; however, other TTL logic families, special functions and gate arrays do not. The QuickSwitch™ can be used to convert these devices to hot plug operation by providing the necessary isolation from the system bus until power is applied to the hot plugged card.

Background

In a hot plug situation, a card is plugged into a system while the system is running. An example of such a system is shown in Figure 1. The card connector is designed so that the ground pin contacts first, followed by the various signal pins and the power pin(s). When the signal pins are connected to the system bus, the logic on the card which has been plugged in will initially be unpowered. In this condition, the logic must guarantee that it will not disturb the system bus when it is unpowered, i.e. that it draws no current from the bus.

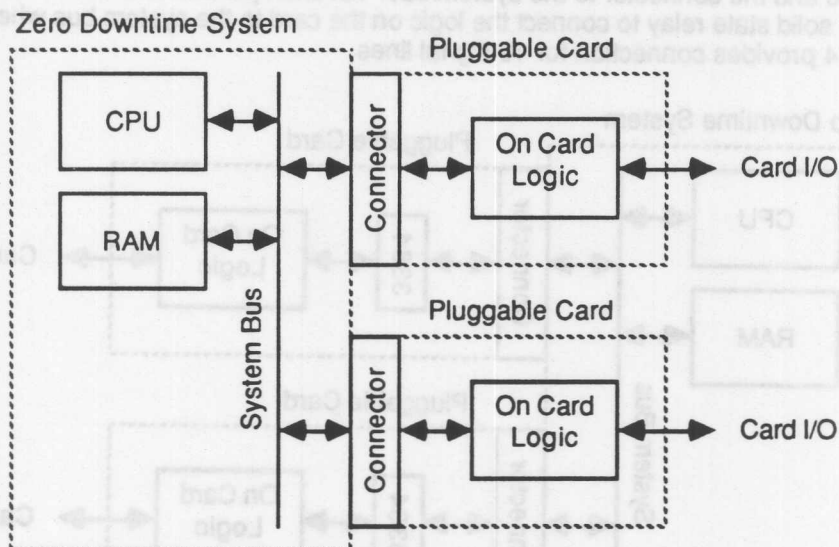


Figure 1: Hot Plug Cards in a Zero Downtime System

Some logic types cannot guarantee that they will not disturb the bus when they are unpowered, for example logic and gate arrays with CMOS outputs. CMOS outputs contain P channel MOS transistors which allow the outputs to be pulled to Vcc for full CMOS levels. These P channel transistors provide an inherent diode between the output and Vcc that is forward biased when the output is driven above Vcc. This means that if the part is powered down, this diode will pull the bus down with it. TTL high signals on the bus will be shunted through this diode to the local Vcc on the card. Since this Vcc goes to all devices on the card as well as large decoupling capacitors, this diode will pull the system bus signals down to approximately one diode drop, 0.7 volts, above ground. This definitely violates the principle of not disturbing the system bus.

Another requirement of hot plugging is that the logic on the hot plugged card does not disturb the bus while the card is being powered up. This means that the logic must remain off as the power on the card transitions from zero to its nominal value, which will typically take several microseconds. If any on-card initialization or self test is required after power up, this activity must also be isolated from the system bus until the card is ready for operation.

As part of the requirement that the hot plugged card does not disturb the system bus, the capacitance of the logic on the card as seen by the system bus must be relatively low. This is so that when the card is plugged and this capacitance is charged up by the bus, the disturbance caused by this charging will not cause a system error. This may be a problem if there are several devices on the hot plugged card that connect to the system bus. In this case, the total capacitance of these devices may be enough to disturb the bus at card plug in.

One solution to the hot plug isolation problem is to put a layer of hot plug rated buffers and transceivers, such as QSI's 74FCTT logic, between the card connector and the logic on the card. This has the disadvantage of introducing additional propagation delay, and this logic must be controlled in the case of bidirectional buses, i.e. each transceiver must know which way the data is flowing.

QuickSwitch™ as a Logic Isolator for Hot Plug Applications.

Another solution is to interpose QuickSwitch™ bus switch devices such as the 74QST3384 between the hot plug card logic and the connector to the system bus. An example of this is shown in figure 2. Each 3384 serves as a solid state relay to connect the logic on the card to the system bus when the card is ready. Each 3384 provides connection for 10 signal lines.

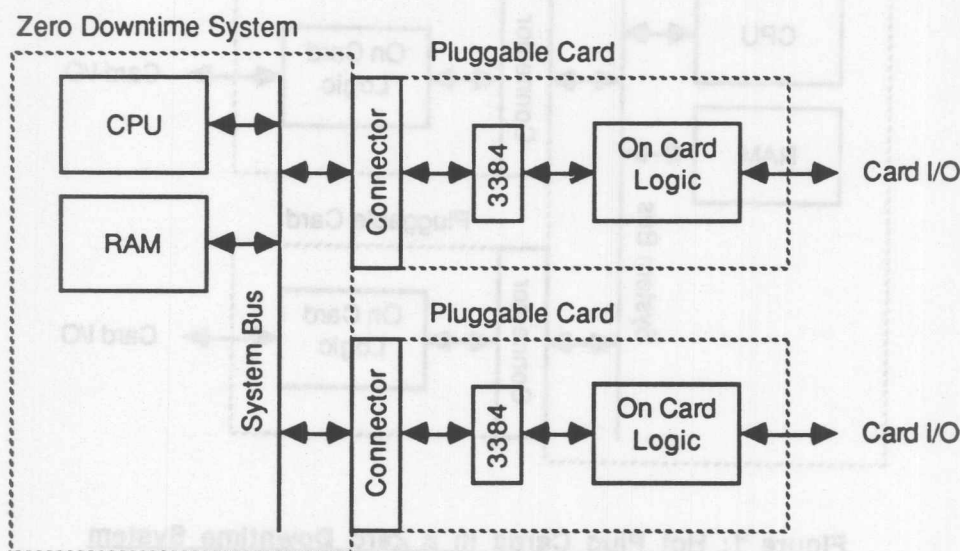


Figure 2: 74QST3384 QuickSwitch™ as Hot Plug Card Isolator

The 3384 QuickSwitch™ devices serve as isolating switches. When they are on, they directly connect the bus on the card to the system bus with an on resistance of 5Ω . When on, these devices act "just like a wire". Like a wire, they introduce negligible delay in the data path and are inherently bidirectional.

It is the off state of the 3384 QuickSwitch™ that is most interesting for hot plug applications. When it is off, it presents low (6 pF) capacitance and a few nanoamperes of leakage to either side of the switch. It is a normally off device, and is off when no power is applied, i.e. Vcc is zero volts. Since the 3384 uses only N channel switches and no P channel devices, there is no diode to Vcc and no current flows when any of the inputs is taken above Vcc. This means that no current flows into the 3384 when it is powered down and connected to an active bus. The 3384 will also remain off during power up until commanded to turn on by asserting the enable lines. (Note: it is recommended that pull up resistors ($10K\Omega$ typical) be added from the 3384 enable inputs to Vcc to hold the 3384's disabled until the logic that drives them is also powered up.)

Once the card has been powered up and any card initialization has been done, the card bus can be connected to the system bus by activating the 3384 enables. The timing of this enable signal can be chosen to provide minimal disturbance when the capacitance of the card bus is connected to the system bus. In fact, the 3384's can be used to selectively connect the card to the bus only when the card is being accessed. This would reduce the capacitance seen by the system bus for operations other than those which access the card.

Figure 3 shows a different version of QuickSwitch™ isolation. In this case, the 3384 isolators are mounted on the backplane. The 3384's remain powered up with the system and are turned on and off as the cards are plugged and unplugged, respectively, from the system. The 3384 enables can be a combination of a ready signal from the card plus a timing signal from the bus indicating a safe time to connect the card.

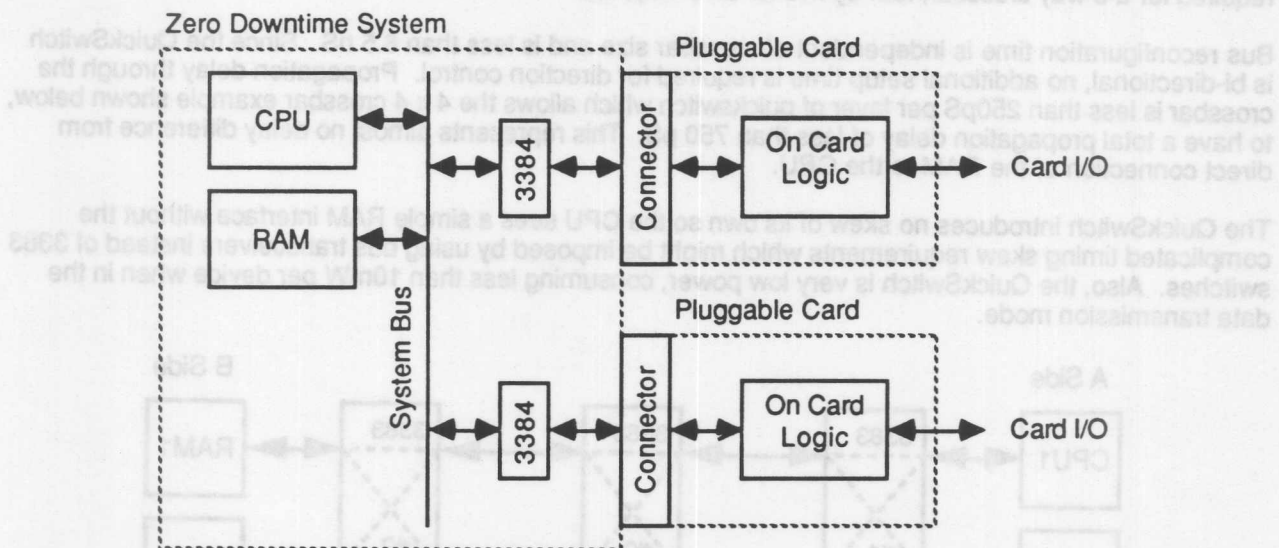


Figure 3: 74QST3384 QuickSwitch™ as System Bus Isolator

Note that it is possible to have 3384's on both the backplane and the hot plugged cards. The 3384's would be in series, like two sets of relay contacts. The system sees a 10Ω resistance rather than 5Ω , and negligible propagation delay between the card and system buses is maintained. Having 3384's on new designs would allow these cards to be added to existing systems, and having 3384's on the backplanes of new systems would allow these new systems to be able to accommodate older design cards which were not designed for hot plugging.

Q

CMOS Bus Exchange Switches for Crossbar Systems

Application
Note
AN-15

by
Mark Muegge

Abstract

Crossbar switches are essential components of high speed data transmission applications such as computer backplanes, LAN's, digital voice, and serial digital video. The QuickSwitch CMOS Bus Exchange Switch by Quality Semiconductor is a high speed TTL bus connect device with nibble swap capability that can be used as a high speed, low power, low cost crossbar switch.

Background

Figure 1 shows the 3383 bus exchange switch used to connect four CPUs and four memories in a crossbar configuration. By appropriate selection of the 3383 bus exchange controls, this configuration provides a non-blocking architecture that makes all memories available to all CPU's, but prevents multiple CPU's from accessing the same memory simultaneously and vice versa. A two by three matrix of 3383 bus exchange switches is required for the four-way crossbar shown below. A three by four matrix will be required for a 6-way crossbar, four by five for an 8-way, etc.

Bus reconfiguration time is independent of crossbar size and is less than 6.5 nS. Since the QuickSwitch is bi-directional, no additional setup time is required for direction control. Propagation delay through the crossbar is less than 250pS per layer of quickswitch which allows the 4 x 4 crossbar example shown below, to have a total propagation delay of less than 750 pS. This represents almost no delay difference from direct connection of the RAM to the CPU.

The QuickSwitch introduces no skew of its own so the CPU sees a simple RAM interface without the complicated timing skew requirements which might be imposed by using bus transceivers instead of 3383 switches. Also, the QuickSwitch is very low power, consuming less than 10mW per device when in the data transmission mode.

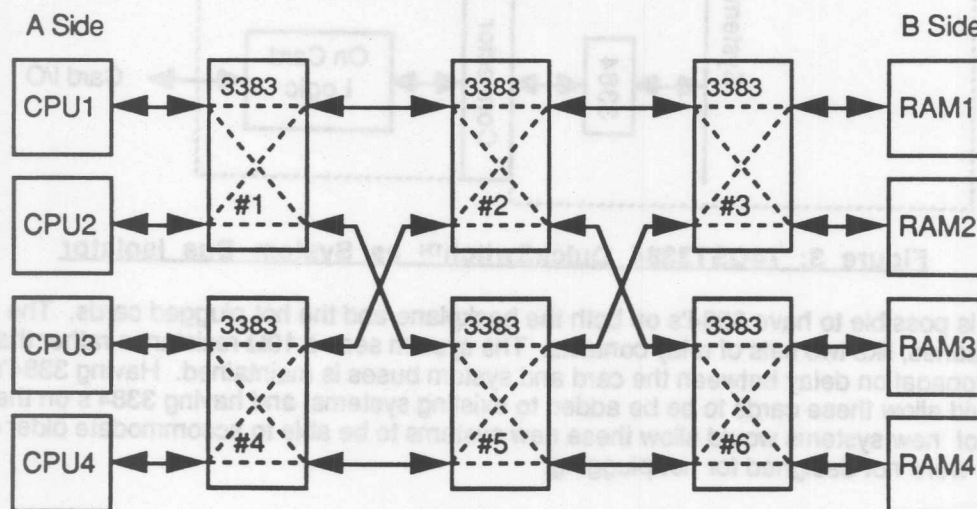


Figure 1: 4 x 4 Crossbar using QuickSwitch

QuickSwitch for Crossbar Is Easy to Use

In the example of the 4 x 4 crossbar switch in figure 1, each 3383 depicted has 5 bit connect/exchange capability. Using the two control pins for each 3383 QuickSwitch (BE for bus enable, BX for bus exchange), it is possible to provide connection from any combination of CPU's to any combination of RAM's, while at the same time not allowing any CPU's to be connected to two RAM's simultaneously or vice versa. The number of possible combinations for a crossbar switch is $N!$ ($1 \times 2 \times 3 \times \dots \times N$) where N equals the size of the crossbar switch. In the example of the 4 x 4 crossbar switch, N equals four. The 24 possible combinations ($1 \times 2 \times 3 \times 4 = 24$) for connecting the four CPU's to the four RAM's of figure 1 are listed below along with the polarity required on each of the QuickSwitches to make the connections.

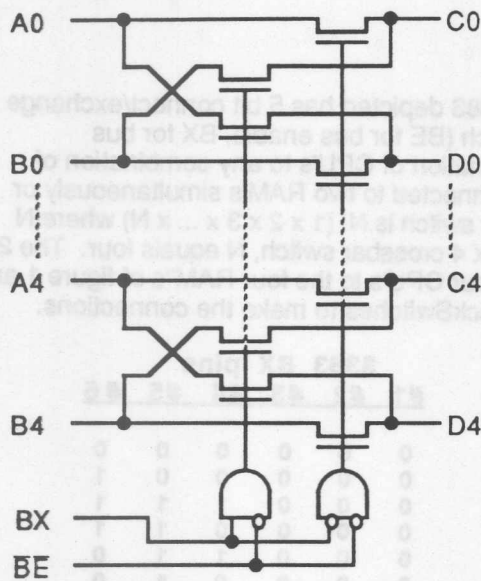
4 x 4 Crossbar Connection Combinations

3383 BX pins #1 #2 #3 #4 #5 #6

A1B1, A2B2, A3B3, A4B4	0	0	0	0	0	0
A1B1, A2B2, A3B4, A4B3	0	0	0	0	0	1
A1B1, A2B3, A3B2, A4B4	0	0	0	1	1	1
A1B1, A2B3, A3B4, A4B2	0	0	0	0	1	1
A1B1, A2B4, A3B2, A4B3	0	0	0	1	1	0
A1B1, A2B4, A3B3, A4B2	0	0	0	0	1	0
A1B2, A2B1, A3B3, A4B4	0	0	1	0	0	0
A1B2, A2B1, A3B4, A4B3	0	0	1	0	0	1
A1B2, A2B3, A3B1, A4B4	1	1	0	0	0	0
A1B2, A2B3, A3B4, A4B1	1	1	0	1	0	0
A1B2, A2B4, A3B1, A4B3	1	1	0	0	0	1
A1B2, A2B4, A3B3, A4B1	1	1	0	0	1	1
A1B3, A2B1, A3B2, A4B4	1	0	0	1	1	1
A1B3, A2B1, A3B4, A4B2	1	0	0	0	1	1
A1B3, A2B2, A3B1, A4B4	1	0	1	1	1	1
A1B3, A2B2, A3B4, A4B1	1	0	1	0	1	1
A1B3, A2B4, A3B1, A4B2	1	1	0	0	1	1
A1B3, A2B4, A3B2, A4B1	1	1	1	0	1	1
A1B4, A2B1, A3B2, A4B3	1	0	0	1	1	0
A1B4, A2B1, A3B3, A4B2	1	0	0	0	1	0
A1B4, A2B2, A3B1, A4B3	1	0	1	1	1	0
A1B4, A2B2, A3B3, A4B1	1	0	1	0	1	0
A1B4, A2B3, A3B1, A4B2	1	1	0	0	1	0
A1B4, A2B3, A3B2, A4B1	1	1	0	1	1	0

QuickSwitch Functions as a High Speed Switch

A block diagram of the 74QST3383 CMOS Bus Exchange Switch is shown in Figure 2. This device consists of two banks of ten switches arranged to gate through or exchange two banks of five signals. This allows the 3384 to be used as a 10-bit switch or as a 5-bit, two way bus exchange device. This part is particularly useful for exchange and routing operations such as byte swap, crossbar matrices, and RAM sharing.



PIN DESCRIPTION

Name	I/O	Function
A0-4, B0-4	I/O	Buses A, B
C0-4, D0-4	I/O	Buses C, D
BE	I	Bus Switch Enable
BX	I	Bus Exchange

FUNCTION TABLE

BE	BX	A0-4	B0-4	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C0-4	D0-4	Connect
L	H	D0-4	C0-4	Exchange

Figure 2: 74QST3383 CMOS Bus Exchange Switch Block Diagram

Each switch consists of an N channel MOS transistor driven by a CMOS gate. When the switch is enabled, the gate of the N channel transistor is at Vcc (+5 volts) and the device is on. These devices have an on resistance of less than 5Ω for voltages near ground and will drive in excess of 64 mA each. The resistance rises somewhat as the I/O voltage rises from a TTL low of 0.0 volts to a TTL high of 2.4 volts. In this region the A and B pins are solidly connected, and the bus switch is specified in the same manner as a TTL device over this range. As the I/O voltage rises to approximately 4.0 volts, the transistor turns off. This corresponds to a typical TTL high of 3.5 to 4.0 volts.

QuickSwitch Provides High Speed Solution

The propagation delay of the QuickSwitch is determined only by the channel resistance and the total load capacitance on the channel. The on resistance of the channel is approximately 5 ohms and the capacitance due to the QuickSwitch is a maximum of 10pF. This gives the QuickSwitch a very low propagation delay. The 250pS maximum propagation delay specified for the 3383 and 3384 assume a total load of 50pF which means that if the system has less than 40pF of capacitance on the QuickSwitch, the actual propagation delay will be even lower. Some high speed data transmission applications require data rates as high as 1 Gbits/S which requires devices with propagation delays of 1nS or less which is easily within the QuickSwitch's capabilities. The QuickSwitch can pass signals with little or no attenuation at data rates as high as 3Gbits/S as shown in Chart 2.

QuickSwitch Frequency Response

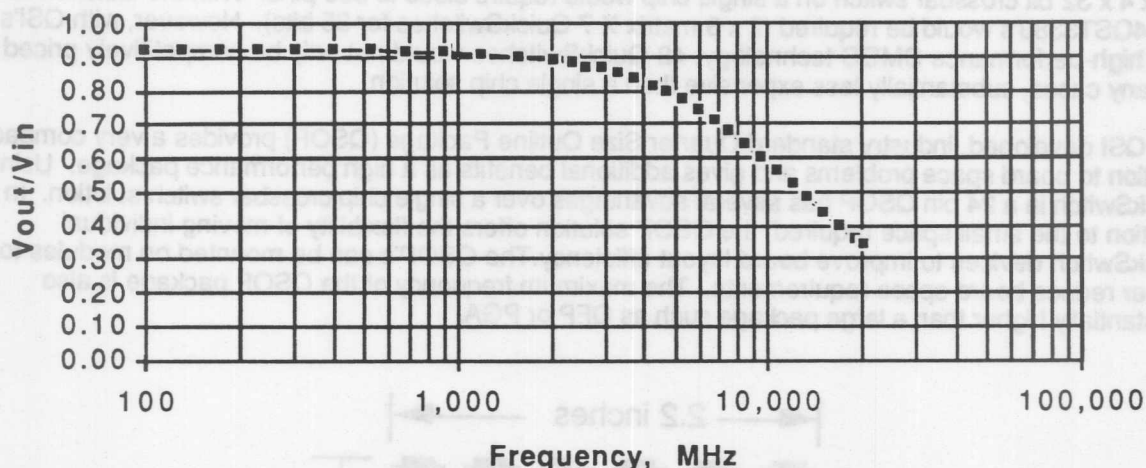


Chart 1: QuickSwitch Attenuation vs. Frequency

It is possible for the QuickSwitch to attain this high performance because it is passing signals, not driving them. The QuickSwitch acts as a solid state relay with a 6.5nS turn-on time and a 5.5nS turn-off time. Because the QuickSwitch has no drive capability, no noise is introduced into the system. The 5 ohm channel resistance actually helps reduce some of the system noise that is present. Figure 2 shows a high speed waveform passed through the QuickSwitch. No crosstalk or groundbounce is present.

QuickSwitch Is Expandable for Wide Applications

The QS74QST3383 QuickSwitch is configured to connect/exchange two 5-bit buses as shown in figure 2. For wider buses, multiple QuickSwitches are necessary. Two Quickswitches are used to get a 10-bit bus, 3 QuickSwitches for a 15-bit bus, etc. For any level of parallel expansion, the control pins for each block of QuickSwitches are tied together. For a 4 x 4 x 32 bit crossbar switch, seven QuickSwitches in parallel would provide 35 available bits and when the seven BE pins are tied together and the seven BX pins are tied together, the seven QuickSwitches act as a single device with only two control pins as shown below.

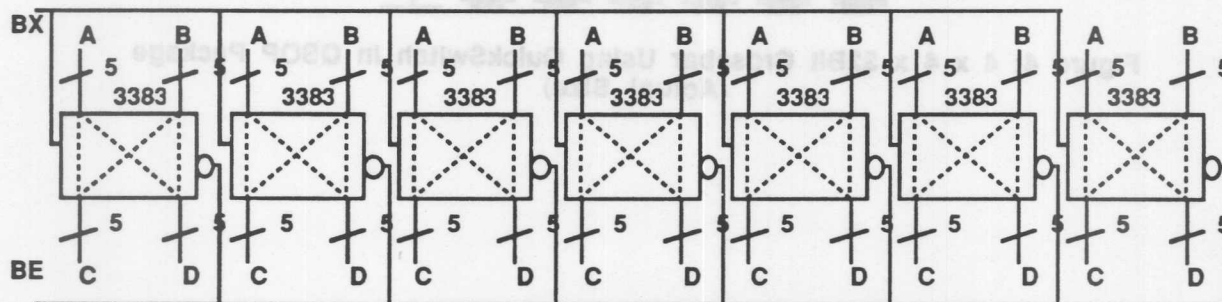


Figure 3: 35 Bit Width Expansion of QuickSwitch

Conclusion

A 4 x 4 x 32 bit crossbar switch on a single chip would require close to 300 pins. With the QuickSwitch, 42 QS74QST3383's would be required (2 x 3 matrix X 7 QuickSwitches for 35 bits). However, with QSI's low cost high-performance CMOS technology, 42 QuickSwitches would not only be competitively priced but in many cases, substantially less expensive than a single chip solution.

The QSI developed, industry standard Quarter Size Outline Package (QSOP) provides a very compact solution to board space problems and gives additional benefits as a high performance package. Using the QuickSwitch in a 24 pin QSOP has several advantages over a single chip crossbar switch solution. In addition to the small space required, the QSOP solution offers the flexibility of moving individual QuickSwitch devices to improve board layout efficiency. The QSOP's can be mounted on modules to further reduce board space requirements. The maximum frequency of the QSOP package is also substantially higher than a large package such as QFP or PGA.

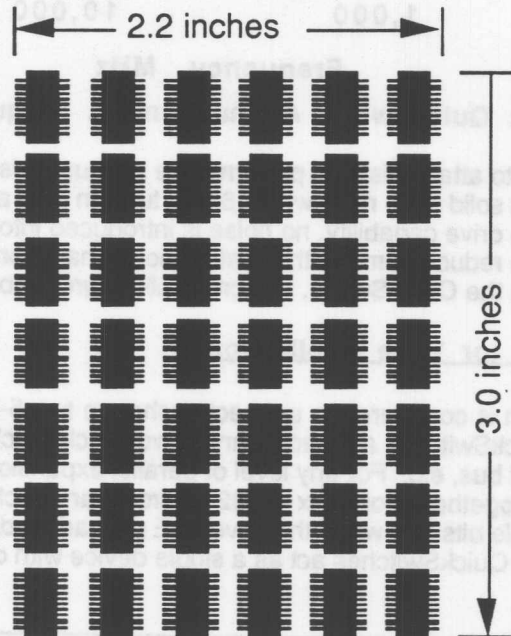


Figure 4: 4 x 4 x 32Bit Crossbar Using QuickSwitch In QSOP Package (Actual Size)

Package Information

PACKAGE INFORMATION

QSI uses a two character package code in the part numbers of its products to indicate the package. The package code is uniform over all part numbers unless otherwise noted. The following is a table of the package codes for some of the packages that house the QuickSwitch product. The package outline drawings for each of these packages is shown on the following pages.

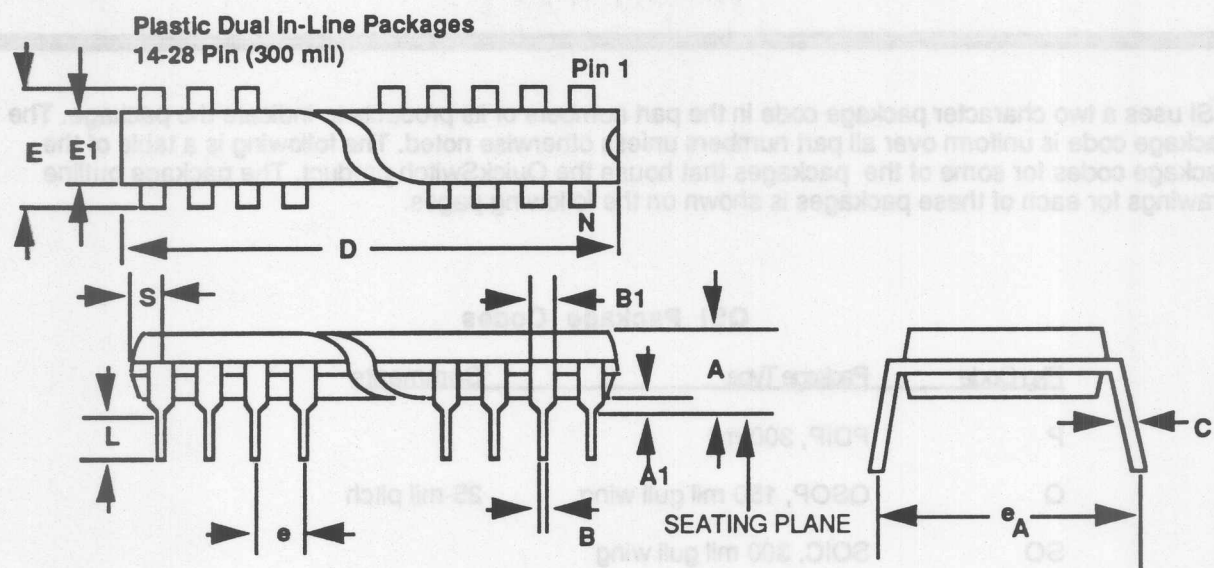
QSI Package Codes

Pkg Code	Package Type	Comments
P	PDIP, 300 mil	
Q	QSOP, 150 mil gull wing	25-mil pitch
SO	SOIC, 300 mil gull wing	
Z	ZIP, zig-zag in-line	

JESD8	MS-001 AC	MS-001 AA	MS-001 AB	MS-001 AC	MS-001 AD	MS-001 AE
DWG#	PD MA	PD MA	PD MA	PD MA	PD MA	PD MA
Symbol	Min	Max	Min	Max	Min	Max
A	.120	.170	.120	.170	.120	.170
A1	.015	.040	.015	.040	.015	.040
B	.018	.050	.018	.050	.018	.050
B1	.045	.070	.045	.070	.045	.070
C	.005	.015	.005	.015	.005	.015
D	.745	.785	.745	.785	.745	.785
E	.300	.325	.300	.325	.300	.325
E1	.240	.270	.240	.270	.240	.270
F	.030	.110	.030	.110	.030	.110
F1	.210	.360	.210	.360	.210	.360
G	.120	.140	.120	.140	.120	.140
H	.010	.050	.010	.050	.010	.050
	14	18	20	22	24	28

Package Information

300 Mil PDIP



Notes:

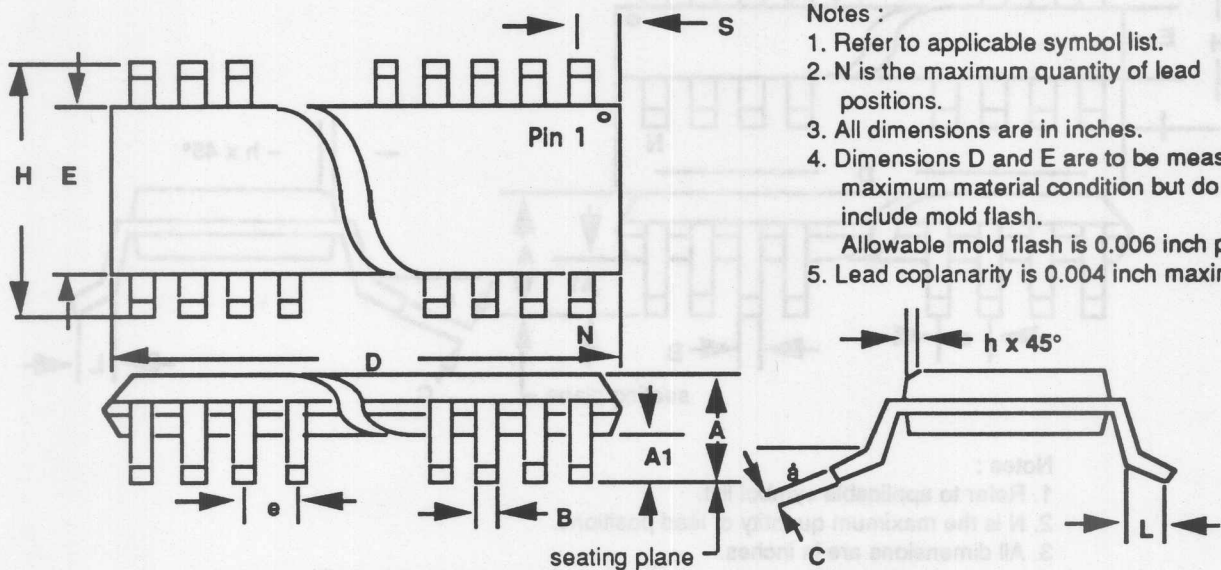
1. Refer to applicable symbol list
2. N is the maximum quantity of lead positions
3. All dimensions are in inches
4. Dimensions D and E1 are to be measured at maximum material condition but do not include mold flash.

JEDEC #	MS-001 AC		MS-001 AA		MS-001 AE		N/A		MS-001 AF		MO-095 AH	
DWG #	PD 14A		PD 16A		PD 20A		PT 22B		PT 24A		PT 28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	.130	.170	.130	.170	.130	.170	.130	.170	.130	.170	.130	.180
A1	.015	.040	.015	.040	.015	.040	.015	.040	.015	.040	.015	.040
B	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020
B1	.045	.070	.045	.070	.045	.070	.045	.070	.045	.070	.045	.060
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.012	.009	.012
D	.745	.765	.745	.765	1.020	1.040	1.020	1.040	1.150	1.260	1.345	1.385
E	.300	.325	.300	.325	.300	.325	.300	.325	.300	.325	.300	.325
E1	.240	.270	.240	.270	.240	.270	.240	.270	.250	.280	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.380	.310	.380	.310	.380	.310	.380	.310	.380	.310	.380
L	.120	.140	.120	.140	.120	.140	.120	.140	.120	.140	.120	.140
S	.070	.080	.020	.035	.060	.070	.010	.020	.025	.080	.020	.040
N	14		16		20		22		24		28	

Package Information

150 MIL QSOP

Quarter Size Outline Package (QSOP) Plastic Small Outline
Gull Wing 16, 20, 24 Pin (150 mil)



Notes :

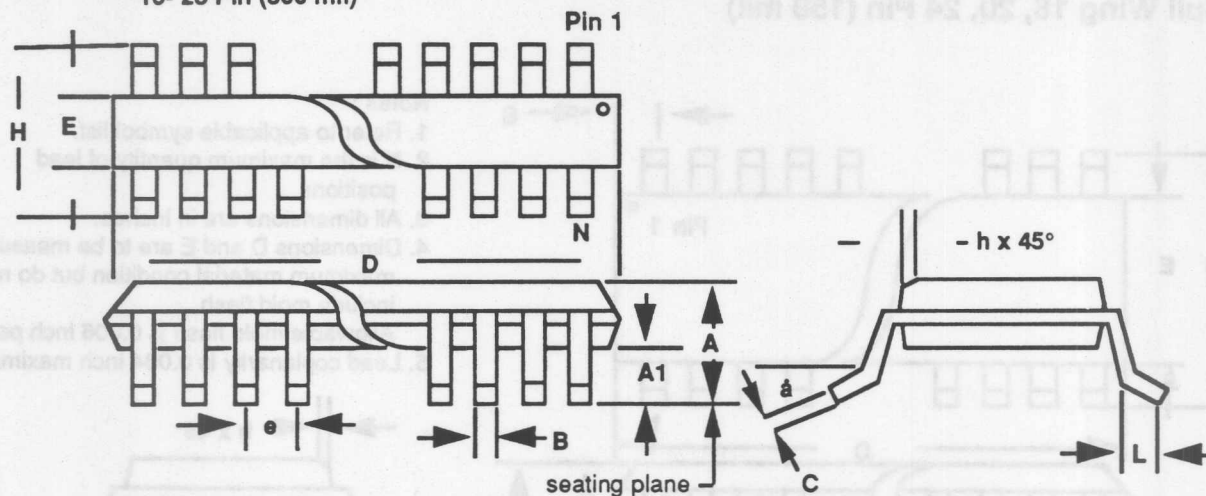
1. Refer to applicable symbol list.
2. N is the maximum quantity of lead positions.
3. All dimensions are in inches.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash.
Allowable mold flash is 0.006 inch per side.
5. Lead coplanarity is 0.004 inch maximum

JEDEC #	TBD			TBD			TBD		
DWG #	PSS-16A			PSS-20A			PSS-24A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.0075	0.008	0.0098	0.0075	0.008	0.0098	0.0075	0.008	0.0098
D	0.189	0.191	0.197	0.337	0.342	0.346	0.337	0.342	0.346
E	0.150	0.155	0.157	0.150	0.155	0.157	0.150	0.155	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24		
a	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.008	0.010	0.056	0.058	0.060	0.031	0.033	0.035

Package Information

300 Mil SOIC

Plastic Small Outline Gull Wing (SOIC)
16- 28 Pin (300 mil)



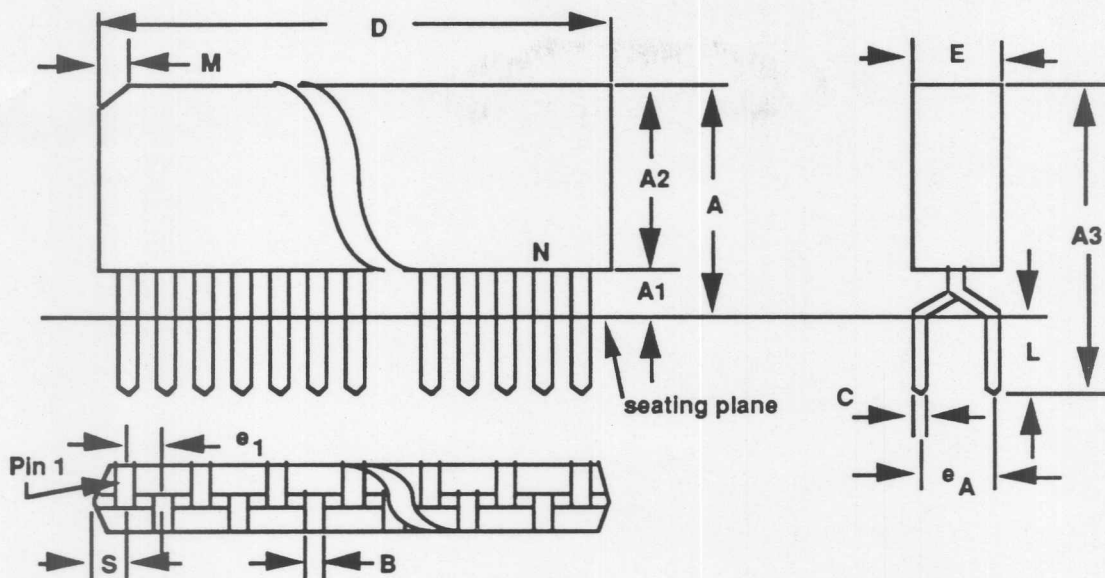
Notes :

1. Refer to applicable symbol list.
2. N is the maximum quantity of lead positions.
3. All dimensions are in inches.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 inch per side.

JEDEC #	MS-013 AA		MS-013 AC		MS-013 AD		MS-013 AE	
DWG #	PS 16A		PS 20A		PS 24A		PS 28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	.096	.104	.096	.104	.096	.104	.096	.104
A1	.005	.011	.005	.011	.005	.011	.005	.011
B	.014	.019	.014	.019	.014	.019	.014	.019
C	.009	.012	.009	.012	.009	.012	.009	.012
D	.402	.412	.500	.510	.602	.612	.701	.711
E	.292	.299	.292	.299	.292	.299	.292	.299
e	.044	.056	.044	.056	.044	.056	.044	.056
H	.396	.416	.396	.416	.396	.416	.396	.416
h	.010	.016	.010	.016	.010	.016	.010	.016
L	.020	.040	.020	.040	.020	.040	.020	.040
N	16		20		24		28	
â	0°	8°	0°	8°	0°	8°	0°	8°

Package Information

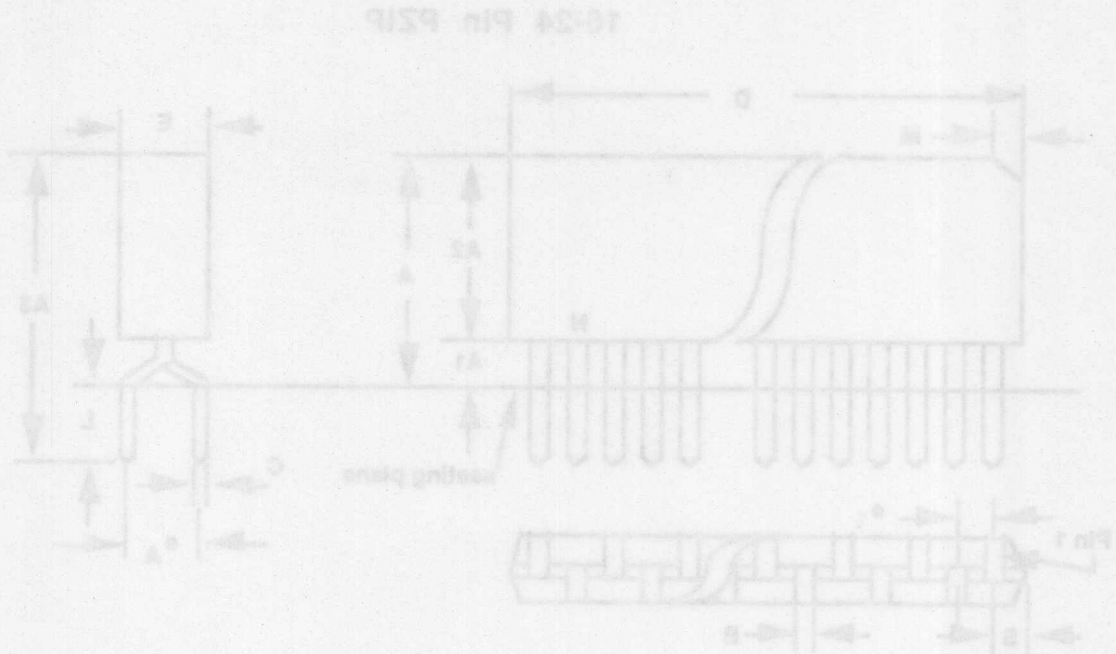
16-24 Pin PZIP



- Notes:**
1. Refer to applicable symbol list.
 2. N is the maximum quantity of lead positions.
 3. All dimensions are in inches.
 4. Dimensions D and A2 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 inch per side.

JEDEC #	MO-054AA		MO-072AB		MO-072AC	
DWG #	PZ 16A		PZ 20A		PZ 24A	
Symbol	Min	Max	Min	Max	Min	Max
A	.290	.350	.350	.400	.350	.400
A1	.060	.100	.030	.070	.030	.070
A2	.250	.270	.280	.340	.320	.350
A3	.390	.500	.450	.550	.450	.550
B	.015	.024	.015	.024	.015	.024
C	.008	.012	.008	.012	.008	.012
D	.786	.814	1.008	1.030	1.200	1.250
E	.100	.120	.100	.120	.100	.120
e1	.050 BSC		.050 BSC		.050 BSC	
eA	.100 BSC		.100 BSC		.100 BSC	
L	.100	.150	.100	.150	.100	.150
M	.035	.085	.035	.085	.035	.085
N	16		20		24	
S	.018	.032	.018	.032	.018	.032

Package Information



Notes: 1. Refer to applicable symbol list.
 2. A1 is the maximum quantity of lead position.
 3. All dimensions are in inches.
 4. Dimensions D and A2 are to be measured in maximum material condition but do not include mold flash. Mold flash is 0.010 inch or less.

JEDEC	16-24 Pin PSIP	16-24 Pin PSIP	16-24 Pin PSIP	16-24 Pin PSIP	16-24 Pin PSIP	16-24 Pin PSIP
DWG	PS 16A	PS 16A	PS 16A	PS 16A	PS 16A	PS 16A
Symbol	Min	Max	Min	Max	Min	Max
A	.280	.280	.280	.280	.280	.280
A1	.080	.100	.080	.100	.080	.100
A2	.280	.280	.280	.280	.280	.280
A3	.280	.280	.280	.280	.280	.280
B	.018	.024	.018	.024	.018	.024
C	.008	.012	.008	.012	.008	.012
D	.708	.814	.708	.814	.708	.814
E	.100	.120	.100	.120	.100	.120
F	.050 BSC	.050 BSC	.050 BSC	.050 BSC	.050 BSC	.050 BSC
G	.100 BSC	.100 BSC	.100 BSC	.100 BSC	.100 BSC	.100 BSC
H	.100	.120	.100	.120	.100	.120
I	.008	.008	.008	.008	.008	.008
J	.008	.008	.008	.008	.008	.008
K	.018	.024	.018	.024	.018	.024
L	.008	.008	.008	.008	.008	.008
M	.008	.008	.008	.008	.008	.008
N	.008	.008	.008	.008	.008	.008
O	.008	.008	.008	.008	.008	.008
P	.008	.008	.008	.008	.008	.008
Q	.008	.008	.008	.008	.008	.008
R	.008	.008	.008	.008	.008	.008
S	.008	.008	.008	.008	.008	.008
T	.008	.008	.008	.008	.008	.008
U	.008	.008	.008	.008	.008	.008
V	.008	.008	.008	.008	.008	.008
W	.008	.008	.008	.008	.008	.008
X	.008	.008	.008	.008	.008	.008
Y	.008	.008	.008	.008	.008	.008
Z	.008	.008	.008	.008	.008	.008